PY32E407 Datasheet

32-bit ARM® Cortex®-M4F Microcontroller

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Features

- Core
  - 32-bit ARM® Cortex® -M4F processor Supports FPU and DSP instructions
  - Frequency up to 170 MHz
- Memories
  - 128 KB bytes of dual bank Flash (Supports Read-While-Write)
  - 144 KB SRAM
- CORDIC
- Reset and supply management
  - 2.3 to 3.6 V
  - Power-on/power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Clock management
  - 16 MHz high-speed internal RC oscillator (HSI16)
  - 48 MHz high-speed internal RC oscillator for dedicated use (HSI48)
  - 40 kHz low-speed internal RC oscillator (LSI)
  - 4 to 32 MHz high-speed external crystal oscillator (HSE)
  - 32.768 kHz low-speed external crystal oscillator (LSE)
  - PLL supports CPU up to 170 MHz
- Low-power mode
  - Sleep, Low-power run, Low-power sleep,Stop and Standby.
  - V_{BAT} supply for RTC and backup registers
- 3 x 12 bit ADC
  - Up to 19 external input channels
  - Input range: 0 to V_{REF+}
  - Single-ended or differential input
  - Supports sampling time and resolution configuration
  - Supports single-shot, continuous, scan and discontinuous conversion modes
  - Temperature sensor
  - Voltage sensor
- 2 x 12-bit DAC
  - Output range: 0 to V_{REF+}
  - Independent output channel
  - Supports Timer and EXTI triggering
- 4 x Fast analog comparators
- 3 x operational amplifiers that can be used in PGA mode,
- 2 x 6-channel DMA controller
  - Supported peripherals: Timer, ADC, DAC, LCDC, UART, I^2C, I^2S, SPI, SDIO, ESMC
- Up to 86 fast I/Os:
  - All mappable on 16 external interrupt vectors
  - Some ports support 5 V-tolerant
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- Up to 23 timers
  - 2 x 16-bit advanced-control timers, with up to 48 x PWM channels, dead time generation and emergency stop
  - 1 x 32-bit, 14 x 16-bit general-purposed timers with up to 4 independent channels for input capture/output comparison.Up to 41 x PWM independent channels,the general-purposed timers also support encoder interfaces using two inputs of quadrature decoders
  - 1 x 16-bit low power timer
  - 2 x 16-bit basic timers can drive the DAC
  - 2 x watchdog timers (Independent and Window)
  - 1 x SysTick timer: 24-bit downcounter
- RTC
- Communication interfaces
  - 3 x UARTs

- 3 x USARTs
- 1 x LPUART
- 4 x I²Cs
- 3 x SPIs
- 1 x ESMC
- 2 x CANs (CAN2.0/CANFD)
- 2 x USB-OTGs
- 1 x Ethernet MAC
- 1 x SDIO
- 1 x IRTIM (Infrared Interface)

- AES and RNG data encryption functions
- Configurable CRC
- 96-bit unique ID (UID)
- Operating temperature -40 to 105 °C
- Packages: LQFP100, LQFP64, LQFP48, QFN32

Content

1. Introduction

The PY32E407 microcontrollers incorporate the high-performance 32-bit ARM® Cortex®-M4F core operating at up to 170 MHz frequency, It is embedded with up to 512 KB Flash and 144 KB SRAM memory. and available in multiple package options. The device integrates hardware acceleration module Cordic, digital encryption module AES, RNG and multiple communication peripherals such as I^2C, SPI, USART, UART, ESMC, USB, CAN, etc., three 12-bit ADCs, two DACs, 23 timers, and one 10/100M Ethernet MAC.

The PY32E407 microcontrollers operates across a temperature range of -40 to 105 °C and a standard voltage range is from 2.3 to 3.6 V. The device provides Sleep,Low power run, Low power sleep,Stop and Standby five low power operating modes, which can meet different low-power applications.

These features make the PY32E407 microcontrollers suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, as well as industrial applications.

Table 1-1 PY32E407 series product features and peripheral counts

Peripherals		PY32E407V1ET7	PY32E407R1ET7	PY32E407C1ET7	PY32E407K1EU7
Flash (KB)		512	512	512	512
SRAM (KB)		144(96+16+32)	144(96+16+32)	144(96+16+32)	144(96+16+32)
Timers	General-purpose	15			
	Advanced-control	2			
	SysTick	1			
	Basic	2			
	LPTIM	1			
	Watchdogs	2			
RTC		1			
Comm. interfaces	USART	3	3	3	3
	UART	3	3	1	1
	LPUART	1	1	1	1
	I^2C	4	4	4	3
	SPI(I^2S)	3(3)	3(3)	3(3)	3(2)
	10/100 ETH	1	1	-	-
	CAN	2	2	2	2
	USBD-OTG	2	2	2	1
	SDIO	1	1	-	-
	ESMC	1	1	1	-
DMA (channels)		2(6)			
GPIO		86	52	38	28
EXTI		16			
Cordic		1			
LCDC		1			
AES RNG		1			
ADC1		1 (14+5)	1 (14+5)	1 (10+5)	1 (6+5)
ADC2		1 (16+3)	1 (16+3)	1 (10+3)	1 (7+3)
ADC3		1 (15+4)	1 (3+4)	1 (3+4)	1 (1+4)
DAC		2(1)	2(1)	2(1)	2(1)
Comparators		4	4	4	3
OPA		3			2
Max. CPU frequency		170 MHz			
Operating voltage		2.3 to 3.6 V			
Operating temperature		-40 to 105 °C			
Packages		LQFP100	LQFP64	LQFP48	QFN32(4*4)

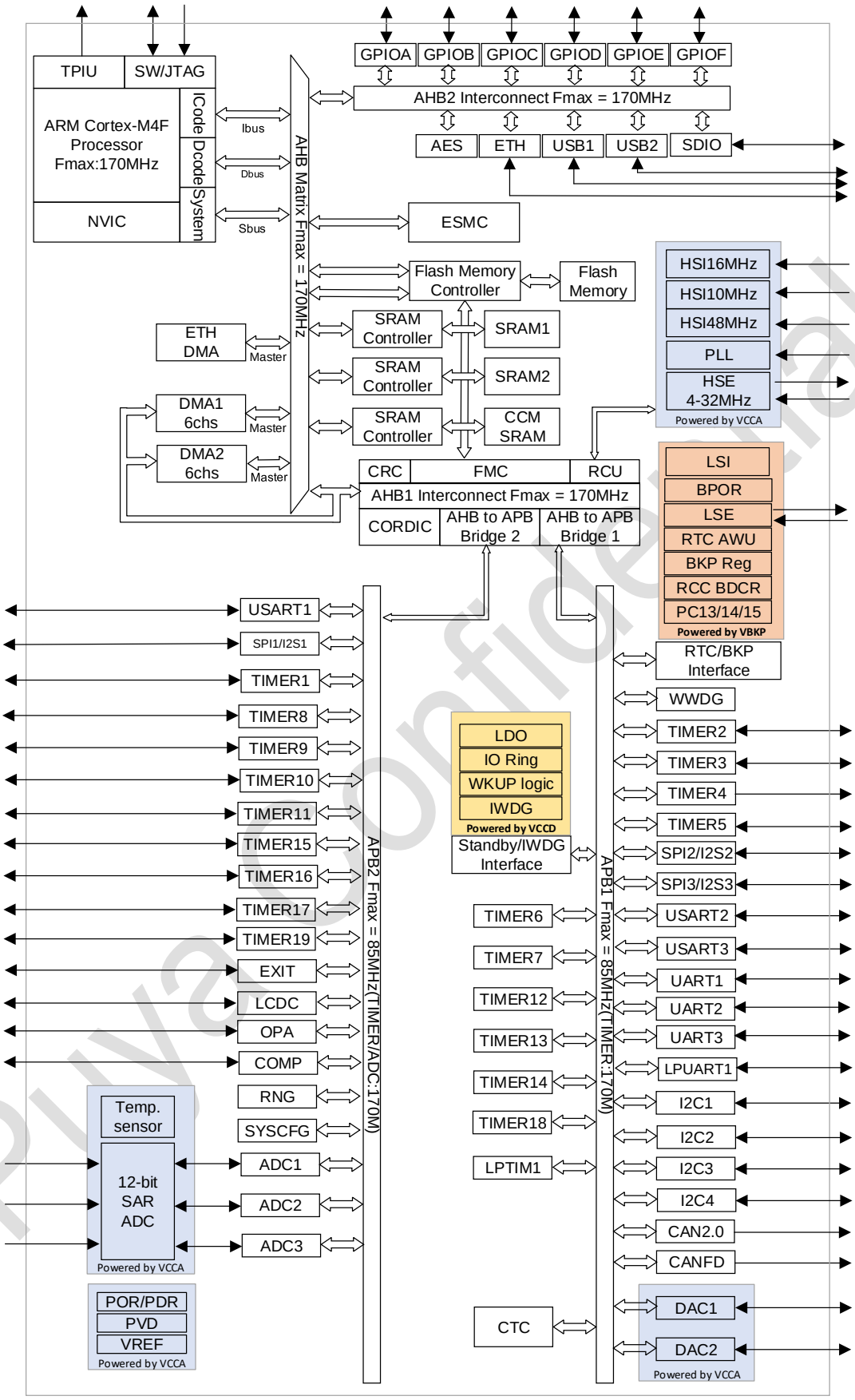


Figure 1-1 System block diagram

2. Functional overview

2.1. ARM® Cortex®-M4F core

ARM® Cortex®-M4F with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices, supporting DSP instructions and FPU floating-point operations. The processor supports a set of DSP instructions, which allow efficient signal processing and complex algorithm execution. Its single-precision FPU (floating-point unit) speeds up software development by using metalanguage development tools, while avoiding saturation. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. It is compatible with all Arm tools and software.

32-bit ARM® Cortex®-M4F processor

- Supports 170 MHz operating frequency
- Single cycle multiplier and hardware divider
- Integrated DSP instructions
- Nested vectored interrupt controller (NVIC)
- 24-bit Sys Tick timer

The ARM® Cortex®-M4F processor is based on the ARMv7-M architecture and supports Thumb and Thumb-2 instruction sets.

- The internal bus matrix connects the I-Code bus, D-Code bus, system bus, private peripheral bus (PPB), and debug access (AHB-AP).
- Nested vectored interrupt controller (NVIC)
- Flash patch and breakpoint (FPB)
- Data watchpoint and trace (DWT)
- Instrumentation trace macrocell (ITM)
- Serial wire JTAG debug port (SWJ-DP)
- Trace port interface unit (TPIU)
- Floating point unit (FPU)
- Memory protection unit (MPU)

2.2. Memories

Embedded up to 144 KB SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The start address of the SRAM is 0x2000 0000.

96 KB SRAM1 (mapped at address 0x2000 0000)

16 KB SRAM2 (mapped at address 0x2001 8000)

32 KB CCM SRAM (mapped at address 0x1000 0000 and end of SRAM2)

when boot fromSRAM1 is selected or when physical remap is selected,it is accessed by the CPU through I-Code/D-Code bus for maximum performance.

The CCM SRAM SRAM mapped at address 0x1000 0000.

Due to accessed by I-Code bus for maximum performance from CCM SRAM without any remapping.

The CCM SRAM succeeds the address at the end SRAM, providing contiguous address space with SRAM and SRAM.

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 32 KB of Information area:
  - Option bytes
  - UID bytes
  - OTP
  - System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.
- Proprietary code readout protection (PCROP)

The Flash memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection

2.3. Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 GB of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and act. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed. The MPU is optional and can be bypassed for applications that do not need it.

2.4. Flash accelerator (ACC)

To release the processor full performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the flash memory. Based on the CoreMark benchmark, the performance achieved thanks to the accelerator is equivalent to 0 wait state program execution from the flash memory at a CPU frequency up to 170 MHz.

- ICODE can prefetch instructions
- The instruction cache has 64 branches and the data bit width is 128 bits
- The data cache has 16 branches, and the data bit width is 128 bits

2.5. Boot modes

At startup, the BOOT0 pin and the boot configuration bit nBOOT0 / nBOOT1 / nSWBOOT0(stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot modes					Mode
BOOT_Lock	nBOOT1 FLASH_OPTR2[8]	nBOOT0 FLASH_OPTR2[14]	BOOT0 Pin PB8	nSWBOOT0 FLASH_OPTR2[13]	
1	X	X	X	X	Boot from Main flash
0	X	X	0	1	Boot from Main flash
0	X	1	X	0	Boot from Main flash
0	0	X	1	1	Boot from SRAM1
0	0	0	X	0	Boot from SRAM1
0	1	X	1	1	Boot from System flash
0	1	0	X	0	Boot from System flash

The Boot loader is located in the system memory and is used to reprogram the Flash memory by using USART, USB, SPI or I^2C interface.

2.6. Backup register (BKP)

Backup registers are 128 8-bit registers used to store 128 bytes of user application data. This module is in the backup domain. When the VDD power is off, they are still powered by V_{BAT}. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode.

- Supports 128-byte data backup register
- Status/control register for managing anti-intrusion detection and having interrupt function
- A check register used to store the RTC check value.
- Output an RTC calibration clock, an RTC alarm pulse or a second pulse on the PC13 pin (when this pin is not used for intrusion detection)

2.7. Clock management

System clock selection is performed on startup, however the internal RC 16 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- An 16 MHz internal high-precision HSI16 clock
- A 48 MHz internal high-precision HSI48 clock can be used to drive the USB
- A 40 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI16, and software configures the HSI16 frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, disable PLL and HSE, and the system clock is automatically switched to HSI16.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The AHB frequency is up to 170 MHz. The APB frequency is up to 85 MHz.

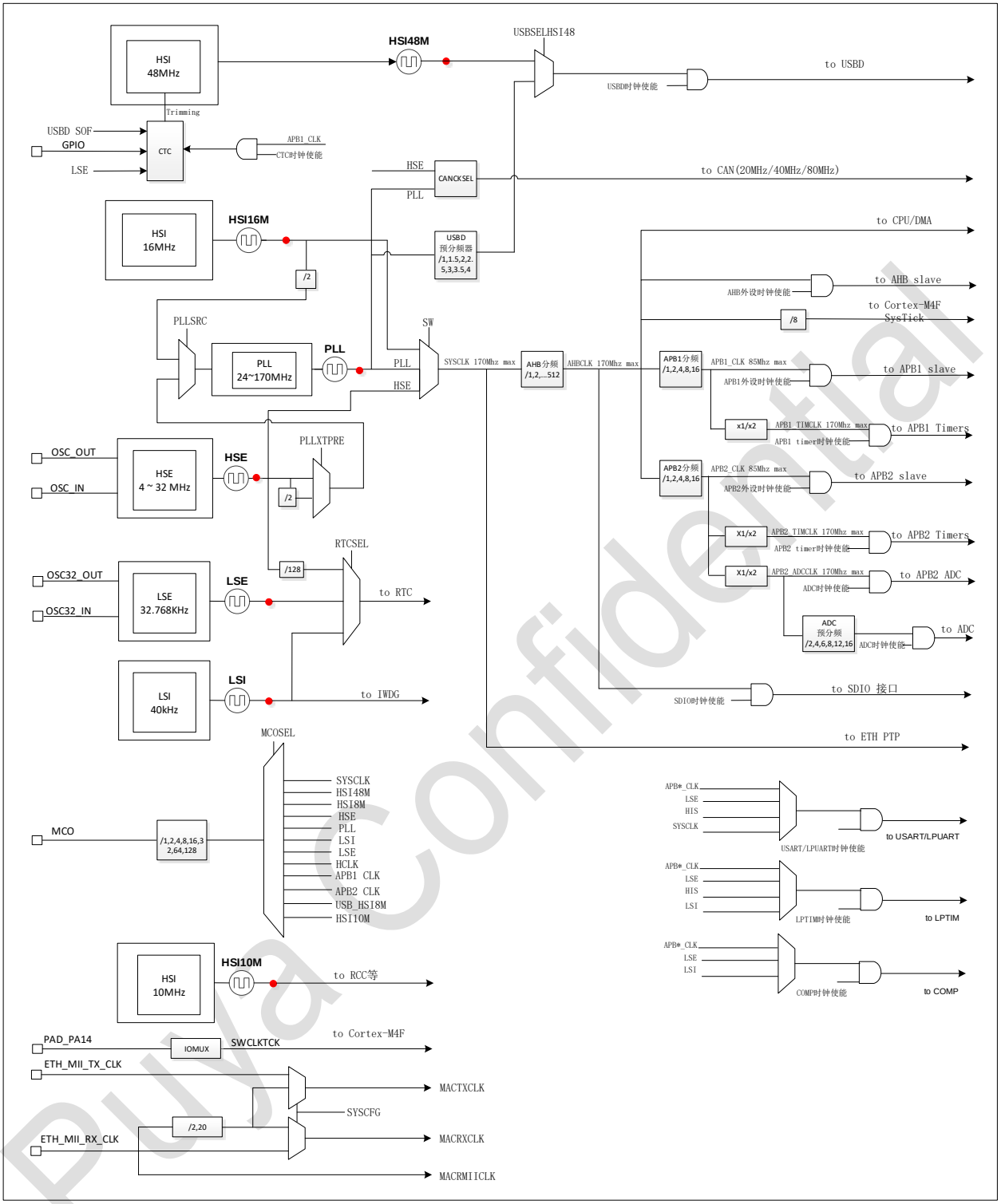


Figure 2-1 System clock structure diagram

2.8. Power management

2.8.1. Power block diagram

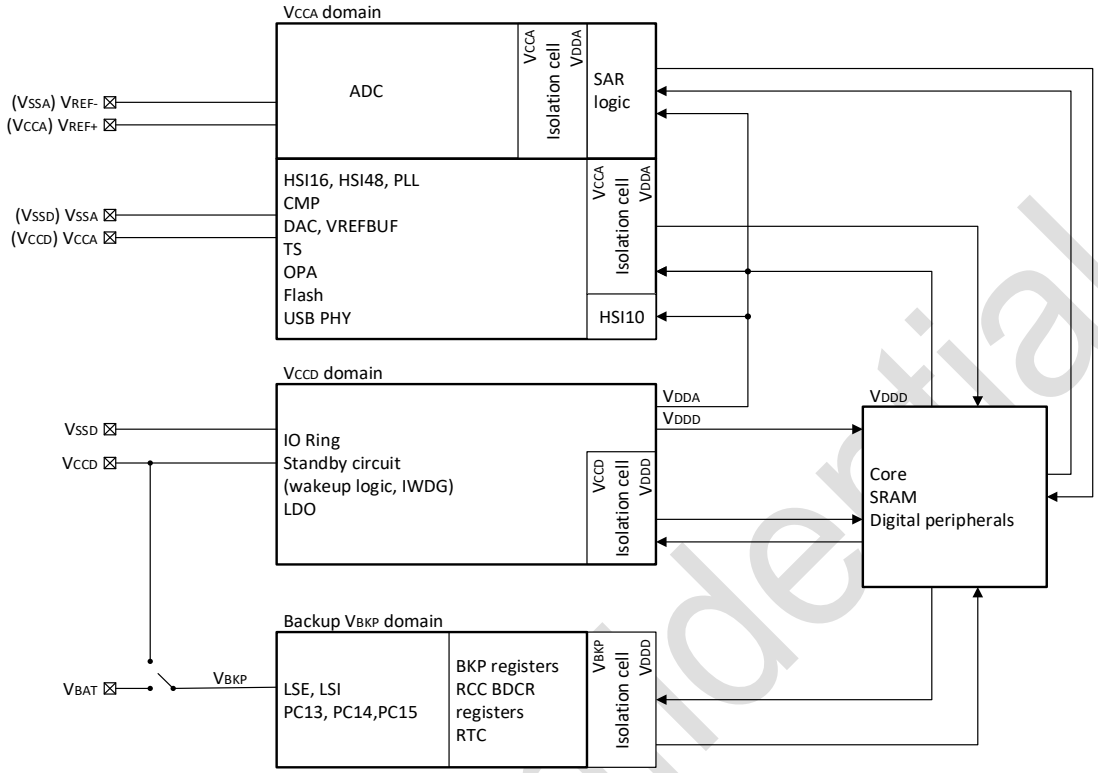


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	2.3 to 3.6 V	The power is supplied to the device through the power pins.
2	V_{CCA}	2.3 to 3.6 V	The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits
3	V_{BAT}	1.65 to 3.6 V	Power supplied for RTC and BKP register.
4	V_{DDX} (V_{DDA}/V_{DDD})	1.1 V	VR supplies power to the main logic circuits and SRAM inside the device.The regulator has two operating modes: **MR (Main regulator):** default 1.1 V power supply, two levels selectable,is used in normal operating mode (Run) and sleep mode. **LPR (Low power regulator):** default 0.9 V power supply, with four selectable levels. is used in Low-power run, Low-power sleep mode In Stop mode, MR or LPR can option. When entering Standby mode, the VR (including MR and LPR) stops working and the V_{DDX} domain is power-down.

2.8.2. Power monitoring

2.8.2.1. Power-on/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed to provide power-on and power-down reset for the device. The module keeps working in all modes.

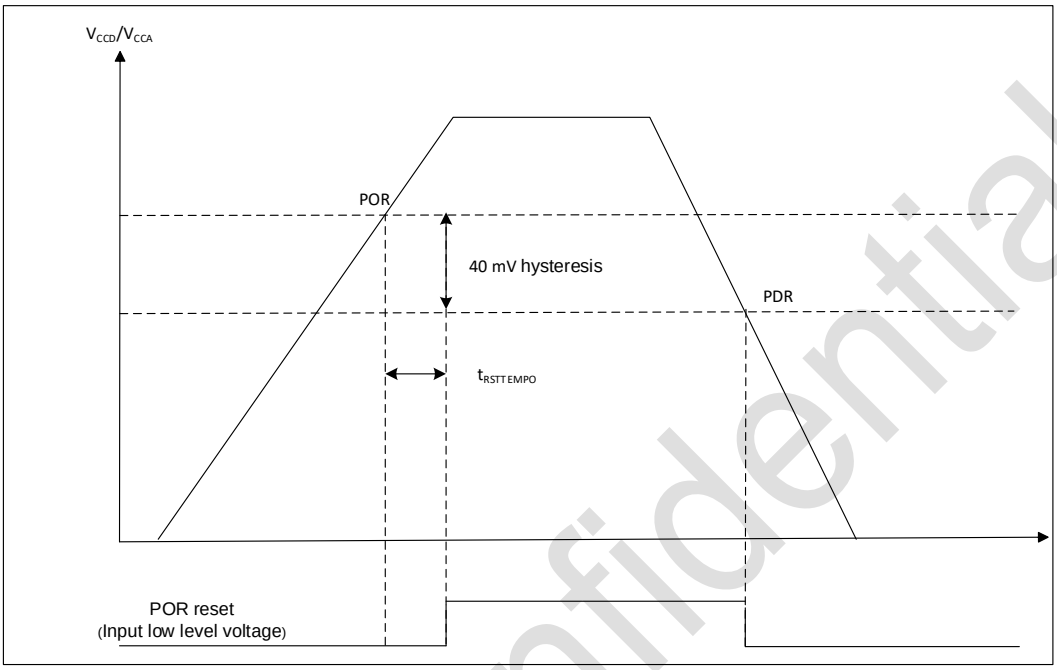


Figure 2-3 POR/PDR thresholds

2.8.2.2. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when VCC rises above the detection point of PVD, or VCC falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

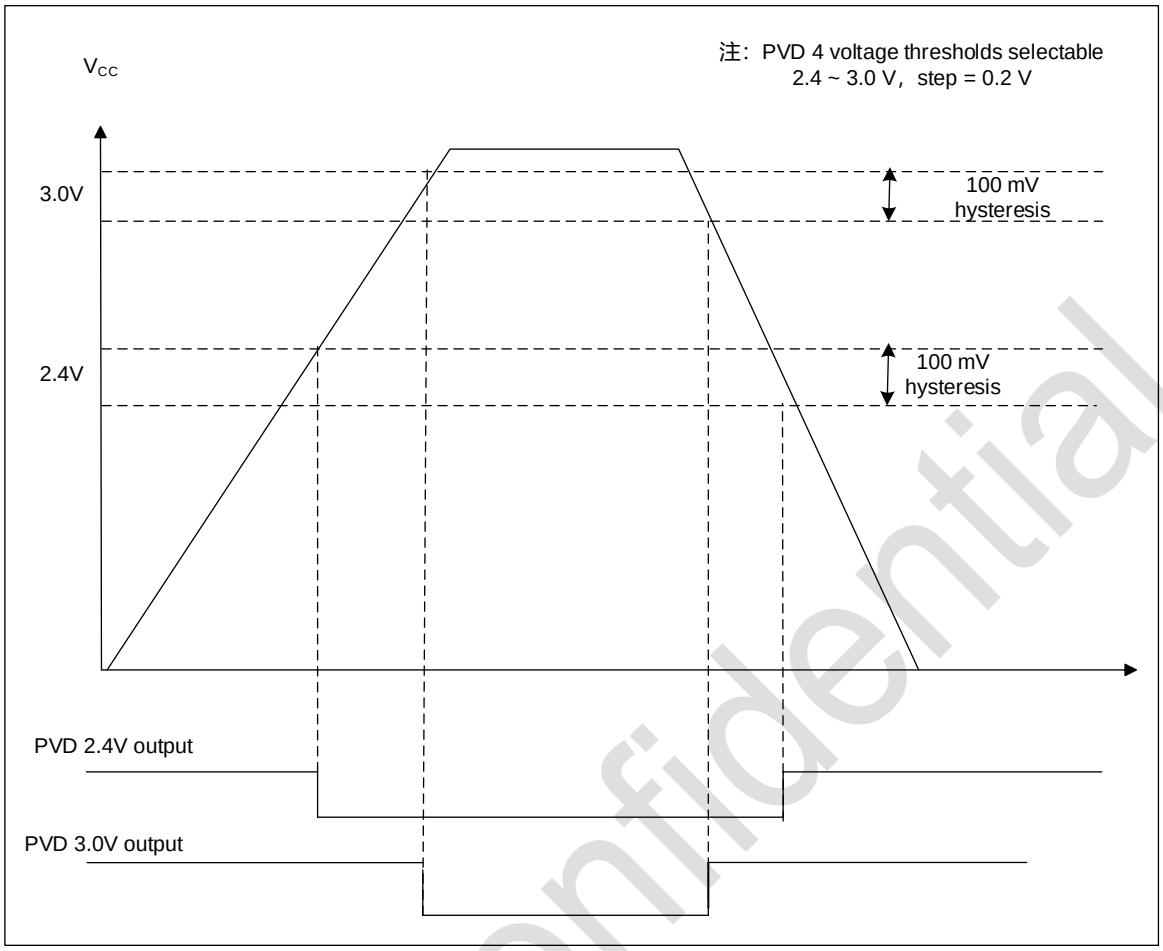


Figure 2-4 PVD threshold

2.8.3. Voltage regulator

The regulator has three operating modes:

- MR (Main regulator) is used in Run mode.
- LPR (Low power regulator) provides an option for even lower power consumption.
- PD (Power-down) where the core power supply is cut off and register and SRAM are lost.

2.8.4. Low-power mode

In addition to the Run mode, the device has five low-power modes:

- **Sleep mode:** Peripherals can be configured to keep working when the CPU clock is off **(**NVIC**,** SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- **Low-power run:** In this mode, the CPU operating frequency is limited to 2 MHz, and peripheral modules with independent clocks can operate at HSI16 frequencies.
- **Low-power sleep mode**: entered only from Low-power run mode and CPU core clock is turned off. The system returns to Low-power run mode when awakened by an event or interrupt.

- **Stop mode**: In this mode**,** SRAM and register contents are retained**.** PLL, HSI16 and HSE are turned off and most module clocks in the V_{DDD} domain are disabled. GPIO, PVD, USB, ETH, I^2C, LPUART, IWDG, Low-power timer,COMP and RTC can wake up the Stop mode.
- **Standby mode:**The V_{DDD} domain is powered off and only the V_{CCD} and V_{BKP} domains work. It can be configured (PWR_CR3.RRS) to select whether or not SRAM2 is power preserved.Exit conditions:external reset via NRST, IWDG reset, RTC alarm wakeup, and valid edge on the WKUP pin.

The device has V_{BAT} power supply, so when the V_{CC} is powered down, the device only works in the V_{BKP} domain.

2.8.5. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Exiting Standby mode

2.8.6. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.9. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up/down, analog) or as peripheral alternate function.The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. OPA features are summarized as follows:

- Support read/write operations via IO Port or AHB bus
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers (Max. 16 alternate functions for each IO)
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions

2.10. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The device has two general-purpose dual-port DMAs (DMA1 and DMA2) with 6 channels respectively. Each channel is dedicated to managing requests for memory access from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- Single AHB Master
- Support peripherals to memory, the memory to the peripherals, memory to memory and peripherals to peripheral data transmission
- On-chip memory devices, such as Flash, an SRAM, AHB and APB peripherals, as the source and target
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
  - The priority between requests is programmable by software (4 levels per channel: very high, high, medium and low) and, in equal cases, by hardware (such as a request for channel 1 taking precedence over a request for channel 2).
  - The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. The source and destination addresses must be aligned by data size.
  - Programmable number of data to be transferred:0 to 65535
- Each channel generates an interrupt request. Each interrupt request is caused by one of three DMA events: transfer completion, half-transfer, or transfer error.

2.11. Interrupts and events

The PY32E407 handles exceptions through the Cortex-M4F processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.11.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M4F processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M4F internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are

listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 86 maskable external interrupts
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.11.2. Extended interrupt/event controller (EXTI)

- EXTI adds flexibility to handle physical wire events and generates wake-up events from GPIO and dedicated modules (PVD/RTC/USB/OTG/ETH/COMP1/COMP2/COMP3/COMP4).
- Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.
- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.12. Trigonometric gas pedal (CORDIC)

CORDIC modules provide hardware acceleration of specific mathematical functions, especially trigonometric functions, commonly used in motor control, metrology, signal processing and many other applications. It speeds up the computation of these functions compared to software implementations, allowing for lower system frequencies or to free up processor to perform other tasks.

- 24-bit CORDIC rotary engine
- Circular and hyperbolic systems
- Rotation and vector modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural, logarithm
- Programmable accuracy
- Low latency AHB interface
- No polling or interrupting, read results when they are ready

- DMA read/write channels
- Read/write multiple registers via DMA

2.13. Analog-to-digital converter (ADC)

- The device has three 12-bit SARADC. Each ADC supports up to 19 conversion channels, with ADC1 has up to 14 external channels and 5 internal channels, ADC2 has up to 16 external channels and 3 internal channels, and ADC3 has up to 15 external channels and 4 internal channels A/D conversion of the various channels can be performed in single,continuous,scan or discontinuous mode.
- A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Interrupt requests are triggered by the following events: end of conversion, continuous conversion and analog watchdog threshold violation (converted voltage exceeds preset limits)
- The ADC is configurable with 12/10/8/6-bit resolutions
- Maximum ADC sampling rate: 4 MSPS
- Supports self-calibration
- Support programmable sampling time
- The data register allows configurable data alignment
- Support DMA requests for regular channel data conversion
- Dual ADC mode (with 2 or more ADC devices)
- Configurable single-ended or differential inputs
- The oversampler is equipped with a 16 - bit data register. The oversampling rate can be adjusted from 2 to 256, and the programmable data shift can reach up to 8 bits
- Data processing supports gain compensation and offset compensation.

2.14. Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The DAC can be configured in 8-bit or 12-bit mode, or can be used in conjunction with a DMA controller. When the DAC is operating in 12-bit mode, the data can be left justified or right justified. The DAC module has two output channels, each with a separate converter. In dual-DAC mode, the two channels can be converted independently, or they can be converted simultaneously and update the output of the two channels synchronously. The DAC can input the reference voltage V_{REF+} through the pin for more accurate conversion results. The main features are as follows:

- Left or right data alignment in 12-bit mode

- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- Support DMA underflow error detection
- External triggers for conversion
- Input voltage reference, V_{REF+}

2.15. Comparators (COMP)

The device integrates four general-purpose comparators (COMP), namely COMP1,COMP2,COMP3 and COMP4. The COMP1/4 module can be used as a separate module or in combination with timer. The comparator can be triggered by analog signals to generate low-power mode wake-up functionality, supports analog signal conditioning, and when connected to PWM outputs from timers, enables cycle-by-cycle current control loops. The main features are as follows:

- Voltage comparison function is supported. Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - 64 steps voltage of V_{CCA}/V_{REFBUF}
  - Temperature sensor output
  - DAC output
- Programmable speed and power consumption
- Rail to Rail
- Programmable hysteresis function
- Write protection for configuration registers (LOCK function)
- The output can be triggered by a connection to the I/O or timer input
- Each COMP has interrupt generation capability and is used to wake up the device from low power mode (Sleep/Stop) (via EXTI)
- Provides software to configure the digital filtering time to enhance the anti-interference capability of the device
- It supports output blanking to reduce switching noise.
- Support the Window Comp function

2.16. Operational amplifier (OPAMP)

Two operational amplifiers are embedded, each has two inputs and one output. Three I/Os can be connected to external pins, enabling any type of external interconnection. operational amplifier can be configured in stand-alone mode (external gain setting mode), and programmable gain amplifier

modes include programmable gain amplifier mode with external filtering, non-inverting or inverting mode with external bias (bias), and non-inverting or inverting mode with external bias with filtering. As an amplifier non-inverting gain ranges from 2 to 32 and inverting gain ranges from -1 to -31.

The positive input can be connected to the internal DAC. The output is connected to the internal ADC. The main features are as follows:

- Rail-to-rail input and output voltage ranges
- Low input bias current
- Low input offset voltage
- High frequency gain bandwidth
- High-speed mode for better conversion rates

2.17. Timer (TIMx)

Table 2-3 Timer characteristics

Timer type	Timers	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	4
	TIM8	16-bit	up, down, up/down	1 to 65536	Yes	4	4
General-purpose	TIM2	32-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM4	16-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM5	16-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM18	16-bit	up, down, up/down	1 to 65536	Yes	4	-
General-purpose	TIM10/ TIM11/ TIM13/ TIM14/TIM19	16-bit	Up	1 to 65536	-	1	-
General-purpose	TIM9/ TIM12	16-bit	Up	1 to 65536	-	2	-
General-purpose	TIM15	16-bit	Up	1 to 65536	Yes	2	1
General-purpose timers	TIM16/TIM17	16-bit	Up	1 to 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	1 to 65536	Yes	-	-

2.17.1. Advanced timers (TIM1/TIM8)

The advanced-control timer (TIM1/TIM8) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, TIM1/TIM8 has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

Two brake input places the output signal of the timer in a safe state.

Add jitter improves the effective resolution of the PWM.

Increasing the index input, the counter is reset by the absolute position index signal indicated by the encoder.

Add PWM combined mode, asymmetric mode and combined three modes.

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the timer link feature for synchronization or event chaining.

TIM1/TIM8 supports DMA function.

2.17.2. General-purpose timers

2.17.2.1. TIM2/TIM3/TIM4/TIM5/TIM18

The general-purpose timers TIM2/TIM3/TIM4/TIM5/TIM18 are consist of 16 bit auto-reload counters driven by a 16-bit (TIM2 is 32-bit)programmable divider. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the Timer Link.
- Support DMA function
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

2.17.2.2. TIM10/ TIM11/ TIM13/TIM14/TIM19

- The general-purpose timers TIM10/TIM11/TIM13/TIM14/TIM19 are consist of 16-bit auto-reload counters and a prescaler.
- TIM10/TIM11/TIM13/TIM14/TIM19 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.17.2.3. TIM9/TIM12

- TIM9 and TIM12 consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM9/TIM12 features two single channels for input capture/output compare, PWM or one-pulse mode output.
- TIM9/TIM12 have complementary outputs with dead time.
- The counter can be frozen in debug mode.

2.17.2.4. TIM15/TIM16/TIM17

- The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload up counter driven by a programmable prescaler.
- TIM15 features 2 (TIM16/TIM17 having one) channels for input capture/output compare, PWM or one-pulse mode output.
- TIM15/TIM16/TIM17 have complementary outputs with dead time.
- Interconnection between timer and timer is controlled by external signal (only supported by TIM15)
- Support DMA function

2.17.3. Basic timers (TIM6/TIM7)

- The basic timer TIM6/TIM7 is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- 16-bit auto-reload counter
- DAC synchronous circuit is triggered.
- Generate interrupt/DMA request on update event (counter overflow).

2.17.4. IWDG

Independent watchdog (IWDG) is integrated in the device, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by independent RC oscillator and can work in Stop and Standby mode.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.17.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.17.6. LPTIM

LPTIM is a 16-bit timer. The ability of LPTIM to wake the system from low-power modes makes it suitable for practical low-power applications. LPTIM introduces a flexible clock scheme that can provide the required functionality and performance while minimizing power consumption.

- 16-bit up counter
- It has a 3-bit prescaler with 8 possible division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Optional clocks include LSE, LSI and APB clock
- Support single-shot and continuous modes

2.17.7. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.18. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- The RTC counter clock source can be LSE, LSI and HSE/128.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.19. Cyclic redundancy check calculation unit (CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- When writing to this register, it serves as an input register, allowing you to input new data for CRC calculation.
- When reading from this register, it returns the result of the previous CRC calculation.

- Each time data is written to the register, the calculation result is a combination of the previous CRC calculation result and the new one (CRC calculation is performed on the entire 32-bit word rather than byte by byte).
- You can reset the register CRC_DR to 0xFFFFFFFF by setting the RESET bit in the register CRC_CR. This operation does not affect the data in the register CRC_IDR
- Support configuration of the initial CRC value
- Support configuration of the CRC polynomial
- Support inverting the input data in units of 8/16/32 bits
- Support output inversion
- The input data bit width supports 8/16/32 bits.
- The polynomial bit width can be configured as 7/8/16/32 bits, which is equivalent to the bit width of the output data

2.20. Clock trimming controller (CTC)

The clock trimming controller (CTC) uses hardware to automatically calibrate the RC crystal oscillator internally configured at 48 MHz and serves as the clock source of the USBD module. The CTC module calibrates the clock frequency of HSI based on an external high-precision reference signal source, and automatically or manually adjusts the calibration value to obtain an accurate PLL 48MHz clock.

The CTC module provides the following functions:

- Three external reference sources: GPIO, LSE clock and USBD_SOF.
- Provide software reference synchronization pulse.
- Hardware calibration automatically, no software operation.
- 16 bits calibration counter with reference source capture and overload capabilities.
- 8 bits clock calibration base value for frequency evaluation and automatic calibration.
- Flag bits and interrupts that indicate the state of clock calibration: calibration success state (CKOKIF), warning state (CKWARNIF), and error state (ERRIF).

2.21. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- Enable and disable I^2C Fm+ mode
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- Analog input channel enable
- Enable and disable Noise filter for all GPIOs
- Enable/disable EXTI (External Interrupt) for all GPIOs
- Dual bank internal Flash Address mapping configuration

- Enable and disable PVD Lock
- Enable and disable Cortex-M4F LOCKUP
- Enable and disable ECC Lock
- SRAM, parity enable and disable for CCM SRAM
- CCM SRAM control (erase, write-protect, etc.)

2.22. Debug support(DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep, Stop and Standby mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Block I^2C1, I^2C2, I^2C3, I^2C4 and SMBUS timeouts when the CPU is in HALT mode
- Block CAN2.0 and CANFD receive register updates when the CPU is in HALT mode
- Assigns tracking pins

The DBG register also provides chip ID encoding. This ID encoding can be accessed by a JTAG or SW debug interface, or by a user program.

2.23. SDIO controller (SDIO)

The SD/SDIO MMC card host interface (SDIO) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards, SDIO cards and the CE-ATA device.

The SDIO features include the following:

- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0
- Full compliance with MultiMediaCard System Specification Version 4.2
- Fully compliance with the CE-ATA digital protocol Rev1.1
- Supports command completion signals and interrupts to the hostprocessor
- Command completion signal disabed

The SDIO does not have an SPI-compatible communication mode and it is supported by either SD I/O-only cards or the I/O portion of combo cards. Some of these commands have no use in SD I/O devices, such as erase commands, and thus are not supported in the SDIO. In addition, several commands are different between SD memory cards and SD I/O cards and thus are not supported in the SDIO. MMC4.1 does not support boot from DDR.

2.24. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multimaster capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

I²C features:

- Multimaster capability: can be master or slave
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
  - Fast Mode Plus (Fm+): up to 1 MHz
- As master
  - Generate clock
  - Generation of start and stop
- As Slave
  - Programmable I²C address detection
  - Dual-address capability that responds to two secondary addresses
  - Discovery of the stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I²C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Support SMBus
- Support low-power modes; wakes up from Stop mode

2.25. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32E407 contains 3 universal synchronous/asynchronous receiver transmitter (USART) and supports ISO7816, LIN and IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Two internal FIFOs for transmitting and receiving data
- Each FIFO can be enabled/disabled by software and has a status flag
- Dual clock domain with PCLK-independent peripheral-specific core clock
- Programmable data sequence, shifting MSB or LSB first
- Programmable data length of 7, 8 or 9 bits
- Configurable stop bits (0.5, 1, 1.5 or 2 bits)
- The transmitter provides a clock for synchronous transmission
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control: RS232, RS485
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance

2.26. Universal asynchronous receivers/transmitter (UART)

The PY32E407 features two Universal Asynchronous Receivers/Transmitters (UARTs):

- Support 5/6/7/8/9-bit serial data

- Support 1/2 STOP bits (1/1.5 STOP bits for 5-bit data)
- Support sending address/data
- Support fixed parity check
- Support break frames
- Detect start bit errors
- Support programmable fractional baud rates
- Support SWAP function
- Support MSB FIRST endianness switching
- Full-duplex asynchronous communication
- NRZ standard format

2.27. Low-power universal asynchronous receivers/transmitters (LPUART)

The PY32E407 features a low power universal asynchronous receivers/transmitters (LPUART):

- Full - duplex asynchronous communication
- NRZ standard mode
- Programmable baud rate
- 32.768 kHz clock with baud rate range 300 - 9600; higher rates need higher clock freq
- Supports transmit and receive FIFO, software can be enabled separately,
- Dual clock domains: PCLK and dedicated kernel clock
- Configurable word length (7/8/9 bits)
- Configurable MSB or LSB first shifting
- Configurable stop bits (1/2 bit)
- Single-wire half-duplex communication
- Support continuous DMA transfer
- Centralized DMA buffering in SRAM for byte reception/transmission
- Independent enable for transmission and reception
- Independent polarity control for Tx/Rx signals
- Interchangeable Tx/Rx pins
- Support hardware RS - 485/modem flow control
- Parity control: generates parity bit on transmission, checks on reception
- Four error detection flags:
- Interrupt sourcrs with flags:
- Support 5/6/7/8/9-bit serial data

2.28. Serial peripheral interface (SPI)

PY32E407 contains 3 SPIs. The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be

configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 Master mode baud rate prescaling factors (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/2$)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Support TI mode
- Interrupt-causing Master mode faults or overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability
- I^2S features:
- 3 x I^2S bus interfaces with sampling rate 8 to 192 kHz
- Support master and slave mode, full duplex and simplex communications

The I^2S bus provides a standard communication interface for digital audio applications over a 3-wire serial line. Three I^2S bus interfaces operate at 16/32 bit resolution in master or slave mode, with pins multiplexed with SPI1/SPI2/SPI3. Support audio sampling frequencies of 8 to 192 kHz, and the accuracy error is less than 0.5%. A DMA controller is available for all I^2S interfaces.

2.29. External serial memory controller (ESMC)

ESMC (External serial memory controller) is a dedicated communication interface for single, dual, quad,dual-quad and octal channels SPI interface memory (NOR Flash, PSRAM, etc.). It can run in either of the following two modes:

- Indirect mode: all operations are performed using the ESMC register
- Memory mapped mode: external Flash memory is mapped to the device address space, and is regarded as internal memory in the system.

Using the dual memory mode, that is, accessing two Qual SPI memories at the same time, you can achieve twice the throughput and storage capacity similar to Octal SPI memory.

- Two functional modes: indirect and memory mapped mode
- Memory mapped mode supports read and write functions
- Supports 8-bit/16-bit command mode
- Can transmit/receive 8 bits simultaneously
- Dual flash mode, which allows simultaneous transmission/reception of 8 bits by accessing two flashes in parallel
- Octal SPI
- Support SDR and DDR
- Fully programmable opcodes for indirect and memory-mapped modes
- Fully programmable frame formats for indirect and memory-mapped modes
- Integrated FIFO for reception and transmission
- Allows 8-bit, 16-bit and 32-bit data access
- DMA channel for indirect mode operation
- Interrupt generation on FIFO operation completion

2.30. Liquid crystal display (LCD) controller

- Supports driving 8080/6800 protocol LCDs
- High flexibility, parameter can be software controlled, compatible with common LCD driver chip
- Simple operation, by writing different registers to send data or commands to the LCD, read the registers to read the LCD data.

2.31. USB-OTG

The PY32E407 device has two USB-OTG full-speed modules with PHY. Compliant with the USB 2.0 specification and OTG 1.3 specification. It has software configurable endpoint settings and supports suspend/wake-up. The USB OTG full-speed controller requires a dedicated 48 MHz clock, which is generated by the HSI48. The main features of the module are:

- 1.25 SRAM used exclusively by the endpoint (not shared with other peripherals)
- 4 bi-directional endpoints
- Built-in HNP/SNP/ID (no other external resistors required)
- For OTG host mode, a power switch is required when a peripheral that requires power is connected
- The SOF output can be used to synchronize an external audio DAC clock in ISO mode.
- According to the USB 2.0 specification, the supported transfer speeds are.
  - Host mode: full speed (PHY does not support low speed)
  - In device mode: full speed

2.32. Controller area network (CAN)

PY32E407 contains one CAN2.0, one CANFD communication interface module.

The Controller Area Network (CAN) bus is a bus standard that can realize the communication between microprocessors or devices without a host. The CAN FD controller follows the CAN bus CAN2.0 (2.0 A, CAN2.0B) and CAN FD protocols.

The CAN bus controller can handle data sending and receiving on the bus. In this product, the CANFD controller has 12 groups of filters. Filters are used to select messages for the application to receive.

The application program in the CAN FD controller can transmit 1 primary transmit buffer (PTB) and 3 secondary transmit buffers (STB) which help to send the sending data to the bus, and the sending scheduler determines the sending order of the mailboxes. The bus data is obtained through three receive buffers (RB). The 3 STBs and 6 RBs can be understood as a 3-stage FIFO and a 6-stage FIFO, and the FIFO is completely controlled by hardware.

The CANFD bus controller also supports Time-trigger communication.

- Full support for CAN2.0A/CAN2.0B/CANFD protocols
- CAN 2.0 supports a maximum communication baud rate of 1Mbit/s
- The baud rate ranges from 1 to 1/32. The baud rate is flexibly configured
- Six receive buffers
  - FIFO mode
  - Error or non-received data does not overwrite stored messages
- One high - priority primary send buffer PTB
- Three sub-send buffers STB
  - FIFO mode
  - Priority arbitration mode
- 16 separate sets of filters
  - Supports 11-bit standard ID and 29-bit extended ID
  - Programmable ID CODE bit and MASK bit
- Both PTB/STB support single transmit mode
- Support silent mode
- Support loopback mode
- Support capturing transmission error types and locating quorum failure locations
- Programmable error warning value
- Support ISO11898-4 time trigger CAN and receive time stamp

2.33. Ethernet controller (Ethernet MAC)

The PY32E407's Ethernet module supports sending and receiving data over Ethernet in accordance with the IEEE 802.3-2002 standard.

The PY32E407 Ethernet module is flexible and adjustable, making it adaptable to a variety of different customer needs. The module supports two standard interfaces to an external Physical Layer (PHY) module: the Media Independent Interface (MII) defined by the IEEE 802.3 protocol and the Reduced Media Independent Interface (RMII). Suitable for various applications such as switches, network interface cards, etc.

The Ethernet module complies with the following standards:

- IEEE 802.3-2002 standard for Ethernet MAC protocols
- IEEE 1588-2002 Standard for Network Precision Clock Synchronization
- AMBA2.0 compliant AHB master/slave port
- RMII standards as defined by the RMII Association

2.34. Encryption module (AES)

AES encrypts or decrypts data using advanced encryption algorithms that are fully compliant with those defined in the FIPS standard.

- Plaintext size: 128 bits
- Key size: 128, 192 and 256 bits
- Encryption/decryption modes: CBC, CFB, OFB, CTR/ICM, XTS
- Authentication mode: CBC-MAC, CMAC
- Encryption and authentication modes: GCM, CCM

2.35. Random number generation (RNG) module

This RNG provides 32-bit random numbers generated by integrated analog circuitry.

2.36. Serial wire debug (SWD)

An ARM SWD interface allows serial debugging tools to be connected to the PY32E407.

3. Pinouts and pin descriptions

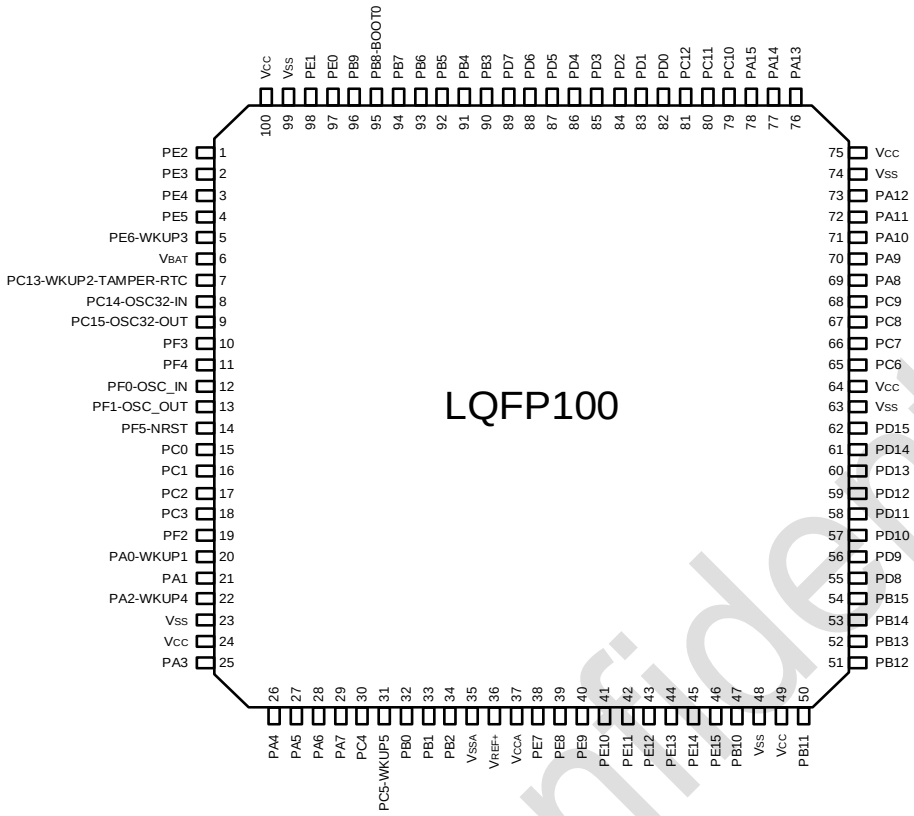


Figure 3-1 LQFP100 Pinout1 PY32E407V1ET7(Top view)

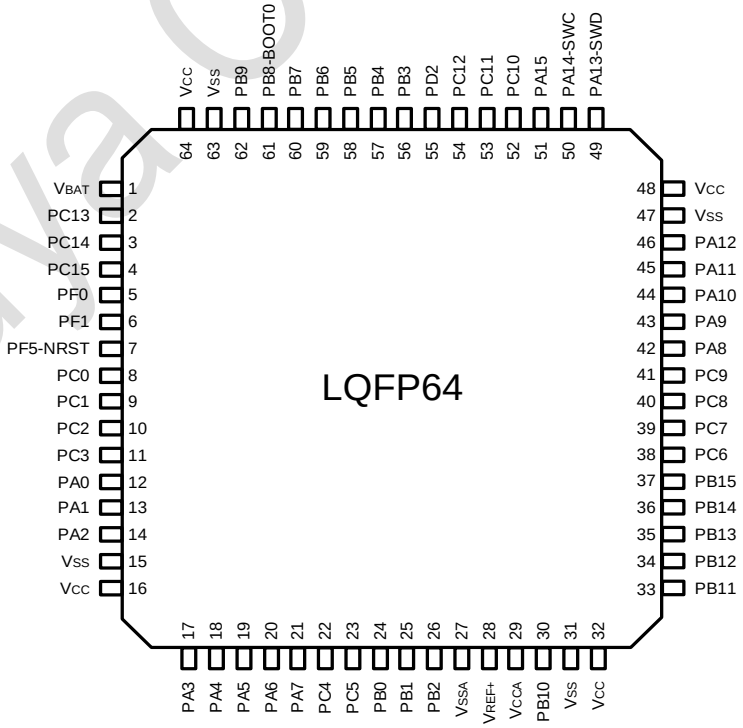


Figure 3-2 LQFP64 Pinout1 PY32E407R1ET7(Top view)

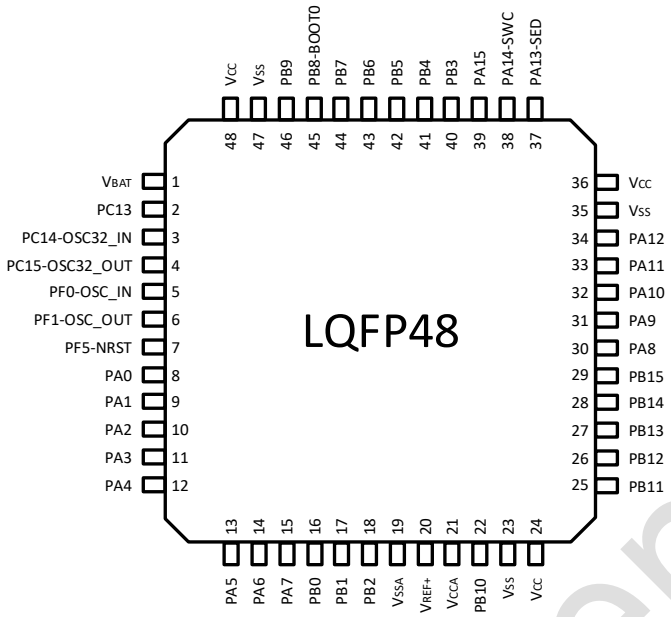


Figure 3-3 LQFP48 Pinout1 PY32E407C1ET7 (Top view)

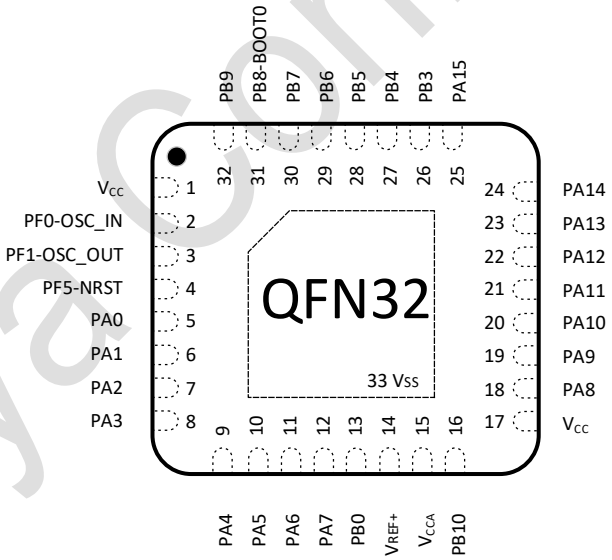


Figure 3-4 QFN32 Pinout1 PY32E407K1EU7 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		NRST	Reset pin, low active
		I/O	Input / output pin
		NC	No internal connection
I/O structure		FT	5 V tolerant I/O
		FT_a	5 V tolerant I/O with Analog switch function
		FT_f	5 V tolerant I/O with I^2C FM+ mode
		FT_fa	5 V tolerant I/O with I^2C FM+ mode and analog switch function
		FT_u	5 V tolerant I/O with USB function
		FT_ua	5 V tolerant with USB and analog switch function
		TT_a	3.3 V tolerant I/O with analog switch function
		TT_fa	3.3 V tolerant I/O with I^2C FM+ mode and analog switch function
		NRST	Reset port with internal weak pull-up resistor
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected or enabled via peripheral registers or option byte

Table 3-2 Pin definitions

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
-	-	-	1	PE2	I/O	FT	TRACECK TIM3_CH1 FDCAN2_RX EVENTOUT	-
-	-	-	2	PE3	I/O	FT	TRACED0 TIM3_CH2 TIM10_CH1 FDCAN2_TX EVENTOUT	-
-	-	-	3	PE4	I/O	FT	TRACED1 TIM3_CH3 TIM9_CH1 LCDC_CS2 EVENTOUT	-
-	-	-	4	PE5	I/O	FT	TRACED2 TIM3_CH4 TIM9_CH2 LCDC_CS3 EVENTOUT	-
-	-	-	5	PE6	I/O	FT	TRACED3 TIM18_CH4 EVENTOUT	WAKEUP3
-	1	1	6	VBAT	S	-	-	-
-	2	2	7	PC13 (2) (3)	I/O	FT	TIM1_BKIN TIM1_CH1N TIM8_CH4N	WAKEUP2 TAMPER

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							EVENTOUT	
-	3	3	8	PC14-OSC32_IN(2)(3)	I/O	FT	EVENTOUT	OSC32_IN
-	4	4	9	PC15-OSC32_OUT(2)(3)	I/O	FT	EVENTOUT	OSC32_OUT
-	-	-	10	PF3	I/O	FT	TIM15_CH1 SPI2_SCK/I2S2_CK TIM5_CH4 TIM12_CH2 ESMC_BK1_IO1 EVENTOUT	-
-	-	-	11	PF4	I/O	FT	TIM15_CH2 SPI2_SCK/I2S2_CK ESMC_CLK LCDC_RS EVENTOUT	-
2	5	5	12	PF0-OSC_IN	I/O	TT_fa	I2C2_SDA SPI2_NSS/I2S2_WS TIM1_CH3N EVENTOUT	ADC1_CH10 OSC_IN
3	6	6	13	PF1-OSC_OUT	I/O	TT_a	SPI2_SCK/I2S2_CK EVENTOUT	ADC2_CH10 COMP3_IN OSC_OUT
5	7	7	14	PF5-NRST	NRST	NRST(FT)	MCO EVENTOUT	NRST
-	-	8	15	PC0	I/O	FT_ua	LPTIM1_IN1 TIM1_CH1 LPUART1_RX ESMC_DQS EVENTOUT	ADC1_CH11/ADC2_CH15 COMP3_INM USB2_OTG_FS_DM

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
-	-	9	16	PC1	I/O	FT_ua	LPTIM1_OUT TIM1_CH2 LPUART1_TX ESMC_BK2_IO0 ETH_MDC EVENTOUT	ADC1_CH7/ ADC2_CH7 COMP3_INP USB2_OTG_FS_DP
-	-	10	17	PC2	I/O	FT_a	LPTIM1_IN2 TIM1_CH3 COMP3_OUT ESMC_BK2_IO1 ETH_MII_TXD2 EVENTOUT	ADC1_CH8/ADC2_CH8 USB2_OTG_FS_ID
-	-	11	18	PC3	I/O	FT_fa	LPTIM1_ETR TIM1_CH4 I2C2_SCL TIM1_BKIN2 ESMC_BK2_IO2 ETH_MII_TX_CLK EVENTOUT	ADC1_CH9/ADC2_CH9 USB2_VBUS
-	-	-	19	PF2	I/O	FT	I2C2_SMBA EVENTOUT	
5	8	12	20	PA0	I/O	TT_a	TIM2_CH1 TIM5_CH1 TIM9_CH1 USART2_CTS COMP1_OUT TIM8_BKIN TIM8_ETR	ADC1_CH1/ADC2_CH1 COMP1_INM/COMP3_INP WAKEUP1

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							TIM19_CH1 TIM11_CH1 ETH_MII_CRS TIM2_ETR EVENTOUT	
6	9	13	21	PA1	I/O	TT_a	TIM2_CH2 TIM5_CH2 TIM9_CH2 USART2_RTS_DE TIM15_CH1N ETH_MII_RX_CLK/ETH_RMII_REF_CLK UART3_RX EVENTOUT	ADC1_CH2/ADC2_CH2 COMP1_INP OPAMP1_VINP/OPAMP3_VINP
7	10	14	22	PA2	I/O	TT_a	TIM2_CH3 TIM5_CH3 TIM12_CH1 TIM18_CH3 USART2_TX COMP2_OUT TIM15_CH1 ESMC_CS0_NCS LPUART1_TX ETH_MDIO UART3_TX EVENTOUT	ADC1_CH3 COMP2_INM OPAMP1_VOUT WAKEUP4
2	-	15	23	V_{SS}	G	-	-	-
1	-	16	24	V_{CC}	S	-	-	-
8	11	17	25	PA3	I/O	TT_a	TIM2_CH4 TIM5_CH4	ADC1_CH4 COMP2_INP

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							TIM12_CH2 TIM18_CH4 USART2_RX TIM15_CH2 ESMC_CLK LPUART1_RX ETH_MII_COL EVENTOUT	OPAMP1_VINM/OPAMP1_VINP
9	12	18	26	PA4	I/O	TT_a	TIM3_CH2 TIM10_CH1 SPI1_NSS/I2S1_WS SPI3_NSS/I2S3_WS USART2_CK ESMC_DQS EVENTOUT	ADC2_CH16 DAC1_OUT COMP1_INM
10	13	19	27	PA5	I/O	TT_a	TIM2_CH1 TIM2_ETR TIM11_CH1 TIM19_CH1 SPI1_SCK/I2S1_CK ESMC_CS2_NCS EVENTOUT	ADC2_CH13 DAC2_OUT COMP2_INM OPAMP2_VINM
11	14	20	28	PA6	I/O	TT_a	TIM16_CH1 TIM3_CH1 TIM13_CH1 TIM8_BKIN SPI1_MISO TIM1_BKIN COMP1_OUT	ADC2_CH3 OPAMP2_VOUT

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							ESMC_BK1_IO3 LPUART1_CTS EVENTOUT	
12	15	21	29	PA7	I/O	TT_a	TIM17_CH1 TIM3_CH2 TIM10_CH1 TIM8_CH1N SPI1_MOSI/I2S1_SD TIM1_CH1N COMP2_OUT ESMC_BK1_IO2 ETH_MII_RX_DV/ETH_RMII_CRS_DV EVENTOUT	ADC2_CH4 COMP2_INP OPAMP1_VINP/OPAMP2_VINP
-	-	22	30	PC4	I/O	TT_a	TIM1_ETR USART1_TX ESMC_BK2_IO3 ETH_MII_RXD0/ETH_RMII_RXD0 EVENTOUT	ADC2_CH5
-	-	23	31	PC5	I/O	TT_a	TIM15_BKIN TIM1_CH4N USART1_RX ESMC_CS1_NCS ETH_MII_RXD1/ETH_RMII_RXD1 EVENTOUT	ADC2_CH11 OPAMP1_VINM/OPAMP2_VINM WAKEUP5
13	16	24	32	PB0	I/O	TT_a	TIM3_CH3 TIM18_ETR TIM8_CH2N TIM1_CH2N ESMC_BK1_IO1	ADC3_CH12/ADC1_CH14 COMP4_INP OPAMP2_VINP/OPAMP3_VINP

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							ETH_MII_RXD2 EVENTOUT	
-	17	25	33	PB1	I/O	TT_a	TIM3_CH4 TIM9_CH1 TIM8_CH3N TIM1_CH3N COMP4_OUT ESMC_BK1_IO0 LPUART1_RTS_DE ETH_MII_RXD3 EVENTOUT	ADC3_CH1/ADC1_CH12 COMP1_INP OPAMP3_VOUT
-	18	26	34	PB2	I/O	TT_a	LPTIM1_OUT TIM5_CH1 TIM18_CH1 I2C3_SMBA ESMC_BK2_IO1 EVENTOUT	ADC2_CH12 COMP4_INM OPAMP3_VINM
-	19	27	35	V_{SSA}	S	-	-	-
14	20	28	36	V_{REF+}(4)	S	-	-	VREFBUF_OUT
15	21	29	37	V_{CCA}	S	-	-	-
-	-	-	38	PE7	I/O	TT_a	TIM1_ETR TIM18_CH3 LCDC_D4 EVENTOUT	ADC3_CH4 COMP4_INP
-	-	-	39	PE8	I/O	TT_a	TIM5_CH3 TIM1_CH1N TIM12_CH1 LCDC_D5	ADC3_CH6 COMP4_INM

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							EVENTOUT	
-	-	-	40	PE9	I/O	TT_a	TIM5_CH4 TIM1_CH1 TIM12_CH2 ESMC_BK1_IO3 LCDC_D6 EVENTOUT	ADC3_CH2
-	-	-	41	PE10	I/O	FT_a	TIM1_CH2N TIM18_CH4 ESMC_CLK LCDC_D7 EVENTOUT	ADC3_CH13
-	-	-	42	PE11	I/O	FT_a	TIM1_CH2 ESMC_CS0_NCS LCDC_D8 EVENTOUT	ADC3_CH14
-	-	-	43	PE12	I/O	FT_a	TIM1_CH3N ESMC_BK1_IO0 LCDC_D9 EVENTOUT	ADC3_CH15
-	-	-	44	PE13	I/O	TT_a	TIM1_CH3 ESMC_BK1_IO1 LCDC_D10 EVENTOUT	ADC3_CH3
-	-	-	45	PE14	I/O	FT	TIM1_CH4 TIM1_BKIN2 ESMC_BK1_IO2 LCDC_D11 EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
-	-	-	46	PE15	I/O	FT	TIM1_BKIN TIM1_CH4N USART3_RX ESMC_BK1_IO0 ESMC_BK1_IO3 LCDC_D12 EVENTOUT	-
16	22	30	47	PB10	I/O	TT_a	TIM2_CH3 USART3_TX LPUART1_RX ESMC_CLK TIM1_BKIN ETH_MII_RX_ER EVENTOUT	OPAMP3_VINM
-	23	31	48	V_{SS}	G	-	-	-
17	24	32	49	V_{CC}	S	-	-	-
-	25	33	50	PB11	I/O	FT_a	TIM2_CH4 USART3_RX LPUART1_TX ESMC_CS0_NCS ETH_MII_TX_EN/ETH_RMII_TX_EN EVENTOUT	ADC1_CH13/ADC2_CH14
	26	34	51	PB12	I/O	TT_a	TIM5_ETR I2C2_SMBA SPI2_NSS/I2S2_WS TIM1_BKIN USART3_CK LPUART1_RTS_DE FDCAN2_RX	ADC1_CH6 OPAMP2_VINP

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							ETH_MII_TXD0/ETH_RMII_TXD0 EVENTOUT	
-	27	35	52	PB13	I/O	TT_a	SPI2_SCK/I2S2_CK TIM1_CH1N USART3_CTS LPUART1_CTS FDCAN2_TX ETH_MII_TXD1/ETH_RMII_TXD1 EVENTOUT	ADC3_CH5 OPAMP3_VINP
-	28	36	53	PB14	I/O	TT_a	TIM15_CH1 SPI2_MISO TIM1_CH2N USART3_RTS_DE COMP4_OUT EVENTOUT	ADC1_CH5
-	29	37	54	PB15	I/O	TT_a	TIM15_CH2 TIM15_CH1N COMP3_OUT TIM1_CH3N SPI2_MOSI/I2S2_SD EVENTOUT	ADC2_CH6
-	-	-	55	PD8	I/O	FT	USART3_TX LCDC_D13 ETH_RMII_CRS_DV EVENTOUT	-
-	-	-	56	PD9	I/O	FT	USART3_RX LCDC_D14 ETH_MII_RXD0/ETH_RMII_RXD0 EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
-	-	-	57	PD10	I/O	FT_a	USART3_CK LCDC_D15 ETH_MII_RXD1/ETH_RMII_RXD1 EVENTOUT	ADC3_CH7
-	-	-	58	PD11	I/O	FT_a	TIM5_ETR I2C4_SMBA USART3_CTS LCDC_D16 ETH_MII_RXD2 EVENTOUT	ADC3_CH8
-	-	-	59	PD12	I/O	FT_a	TIM4_CH1 USART3_RTS_DE LCDC_D17 ETH_MII_RXD3 EVENTOUT	ADC3_CH9
-	-	-	60	PD13	I/O	FT_a	TIM4_CH2 TIM18_CH2 EVENTOUT	ADC3_CH10
-	-	-	61	PD14	I/O	TT_a	TIM4_CH3 LCDC_D0 EVENTOUT	ADC3_CH11 OPAMP2_VINP
-	-	-	62	PD15	I/O	FT	TIM4_CH4 SPI2_NSS/I2S2_WS LCDC_D1 EVENTOUT	-
-	-	-	63	V_{SS}	G	-	-	-
-	-	-	64	V_{CC}	S	-	-	-
-	-	38	65	PC6	I/O	FT_f	TIM3_CH1	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							TIM13_CH1 TIM8_CH1 I2S2_MCK I2C4_SCL ESMC_CS3_NCS SDIO_D6 EVENTOUT	
-	-	39	66	PC7	I/O	FT_f	TIM3_CH2 TIM10_CH1 TIM8_CH2 I2S3_MCK I2C4_SDA SDIO_D7 EVENTOUT	-
-	-	40	67	PC8	I/O	FT_f	TIM3_CH3 TIM18_CH1 TIM8_CH3 I2C3_SCL SDIO_D0 EVENTOUT	-
-	-	41	68	PC9	I/O	FT_f	TIM3_CH4 TIM8_CH4 TIM8_BKIN2 I2C3_SDA -SDIO_D1 LCDC_CS3 EVENTOUT	-
18	30	42	69	PA8	I/O	FT_f	MCO TIM14_CH1	USB1_OTG_FS_SOF

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							I2C3_SCL TIM18_CH1 I2C2_SDA I2S2_MCK TIM1_CH1 USART1_CK TIM4_ETR EVENTOUT	
19	31	43	70	PA9	I/O	FT_fa	I2C3_SMBA TIM18_ETR I2C2_SCL I2S3_MCK TIM1_CH2 USART1_TX TIM15_BKIN TIM2_CH3 LCDC_CS1 EVENTOUT	USB1_VBUS
20	32	44	71	PA10	I/O	FT	TIM17_BKIN CTC_SYNC I2C2_SMBA SPI2_MISO TIM1_CH3 USART1_RX TIM2_CH4 TIM8_BKIN LCDC_CS2 EVENTOUT	USB1_OTG_FS_ID
21	33	45	72	PA11	I/O	FT_u	SPI2_MOSI/I2S2_SD	USB1_OTG_FS_DM

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							TIM1_CH1N USART1_CTS COMP1_OUT FDCAN1_RX TIM4_CH1 TIM1_CH4 TIM1_BKIN2 EVENTOUT	
22	34	46	73	PA12	I/O	FT_u	TIM16_CH1 TIM8_CH4 TIM1_CH2N USART1_RTS_DE COMP2_OUT FDCAN1_TX TIM4_CH2 TIM1_ETR EVENTOUT	USB1_OTG_FS_DP
-	35	47	74	V_{SS}	G	-	-	-
-	36	48	75	V_{CC}	S	-	-	-
23	37	49	76	PA13	I/O	FT_f	SWDIO_JTMS TIM16_CH1N I2C4_SCL I2C1_SCL IR_OUT USART3_CTS TIM4_CH3 LCDC_RS EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
24	38	50	77	PA14	I/O	FT_f	SWCLK_JTCK LPTIM1_OUT I2C4_SMBA I2C1_SDA TIM8_CH2 TIM1_BKIN USART2_TX TIM18_CH2 LCDC_8RD_6RW EVENTOUT	-
25	39	51	78	PA15	I/O	FT_f	JTDI TIM2_CH1 TIM8_CH1 TIM18_ETR I2C1_SCL SPI1_NSS/I2S1_WS SPI3_NSS/I2S3_WS USART2_RX TIM1_BKIN LCDC_8WR_6E TIM11_CH1 TIM19_CH1 TIM2_ETR EVENTOUT	-
-	-	52	79	PC10	I/O	FT	TIM8_CH1N UART1_TX SPI3_SCK/I2S3_CK USART3_TX ESMC_CS4_NCS	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							SDIO_D2 LCDC_CS0 EVENTOUT	
-	-	53	80	PC11	I/O	FT_f	TIM8_CH2N UART1_RX SPI3_MISO USART3_RX I2C3_SDA SDIO_D3 LCDC_D0 EVENTOUT	-
-	-	54	81	PC12	I/O	FT	TIM5_CH2 TIM9_CH2 TIM18_CH2 TIM8_CH3N UART2_TX SPI3_MOSI/I2S3_SD USART3_CK SDIO_CK EVENTOUT	-
-	-	-	82	PD0	I/O	FT	TIM8_CH4N FDCAN1_RX LCDC_D2 EVENTOUT	-
-	-	-	83	PD1	I/O	FT	TIM8_CH4 TIM8_BKIN2 FDCAN1_TX LCDC_D3 EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
-	-	55	84	PD2	I/O	FT	TIM3_ETR TIM8_BKIN UART2_RX ESMC_CS5_NCS SDIO_CMD EVENTOUT	-
-	-	-	85	PD3	I/O	FT	TIM2_CH1/TIM2_ETR USART2_CTS ESMC_CS1_NCS EVENTOUT	-
-	-	-	86	PD4	I/O	FT	TIM2_CH2 USART2_RTS_DE ESMC_BK2_IO0 LCDC_8RD_6RW EVENTOUT	-
-	-	-	87	PD5	I/O	FT	USART2_TX ESMC_BK2_IO1 LCDC_8WR_6E EVENTOUT	-
-	-	-	88	PD6	I/O	FT	TIM2_CH4 USART2_RX ESMC_BK2_IO2 LCDC_CS1 EVENTOUT	-
-	-	-	89	PD7	I/O	FT	TIM2_CH3 USART2_CK ESMC_BK2_IO3 LCDC_CS0 EVENTOUT	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
26	40	56	90	PB3	I/O	FT	JTDO_TRACESWO TIM2_CH2 TIM4_ETR TIM18_CH3 TIM8_CH1N SPI1_SCK/I2S1_CK SPI3_SCK/I2S3_CK USART2_TX CTC_SYNC TIM3_ETR LCDC_D1 EVENTOUT	-
27	41	57	91	PB4	I/O	FT	JTRST TIM16_CH1 TIM3_CH1 TIM13_CH1 TIM8_CH2N SPI1_MISO SPI3_MISO USART2_RX TIM17_BKIN LCDC_D2 EVENTOUT	-
28	42	58	92	PB5	I/O	FT_f	TIM16_BKIN TIM3_CH2 TIM8_CH3N I2C1_SMBA SPI1_MOSI/I2S1_SD SPI3_MOSI/I2S3_SD	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							USART2_CK I2C3_SDA FDCAN2_RX TIM17_CH1 LPTIM1_IN1 LCDC_D3 ETH_PPS_OUT USB2_OTG_FS_SOF EVENTOUT	
29	43	59	93	PB6	I/O	FT	TIM16_CH1N TIM4_CH1 TIM10_CH1 TIM8_CH1 TIM8_ETR USART1_TX COMP4_OUT FDCAN2_TX TIM8_BKIN2 LPTIM1_ETR LCDC_D4 EVENTOUT	-
30	44	60	94	PB7	I/O	FT_f	TIM17_CH1N TIM4_CH2 I2C4_SDA I2C1_SDA TIM8_BKIN USART1_RX COMP3_OUT TIM3_CH4	PVD_IN

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							LPTIM1_IN2 LCDC_D5 EVENTOUT	
31	45	61	95	PB8-BOOT0	I/O	FT_f	TIM16_CH1 TIM4_CH3 I2C1_SCL LCDC_D6 USART3_RX COMP1_OUT FDCAN1_RX TIM8_CH2 SDIO_D4 TIM1_BKIN ETH_MII_TXD3 EVENTOUT	-
32	46	62	96	PB9	I/O	FT_f	TIM17_CH1 TIM4_CH4 TIM14_CH1 I2C1_SDA IR_OUT USART3_TX COMP2_OUT FDCAN1_TX TIM8_CH3 SDIO_D5 TIM1_CH3N LCDC_D7 EVENTOUT	-
-	-	-	97	PE0	I/O	FT	TIM4_ETR	-

Packages				Pin name	Pin type	I/O structure	Port function(1)	
QFN32 K1	LQFP48 C1	LQF64 R1	LQFP100 V1				Alternate functions	Additional functions
							TIM16_CH1 USART1_TX FDCAN1_RX EVENTOUT	
-	-	-	98	PE1	I/O	FT	TIM14_CH1 TIM17_CH1 USART1_RX FDCAN1_TX EVENTOUT	-
-	47	63	99	V_{SS}	G	-	-	-
-	48	64	100	V_{CC}	S	-	-	-

1. Available functions depend on the specified device. If multiple peripherals share the same I/O pin, to avoid conflicts between these functions, only one peripheral can be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
2. The PC13, PC14, and PC15 are supplied through a power switch. The switch is current-limited (3 mA sourcing), thus GPIO PC13 to PC15 output mode have restrictions:
   1) Maximum rate 2 MHz, load ≤30 pF.
   2) Cannot be used as current sources (e.g., LED driving).
3. The main functions after the first backup domain is powered on. After this it depends on the contents of the backup registers, even after a reset (as these registers are not controlled by the main area reset).
4. When using the V_{REFBUF} function, V_{REF+} requires an external 1 µF capacitor.

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TIM2_CH1	TIM5_CH1	TIM9_CH1	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	TIM19_CH1	TIM11_CH1	ETH_MII_CRS	TIM2_ETR	EVENTOUT
PA1	-	TIM2_CH2	TIM5_CH2	TIM9_CH2	-	-	-	USART2_RTS_DE	-	TIM15_CH1N	-	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	UART3_RX	EVENTOUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM12_CH1	TIM18_CH3	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	ESMC_CS0_NCS	-	LPUART1_TX	ETH_MDIO	UART3_TX	EVENTOUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM12_CH2	TIM18_CH4	-	-	USART2_RX	-	TIM15_CH2	ESMC_CLK	-	LPUART1_RX	ETH_MII_COL	-	EVENTOUT
PA4	-	-	TIM3_CH2	TIM10_CH1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	ESMC_DQS	-	-		-	EVENTOUT
PA5	-	TIM2_CH1	TIM2_ETR	TIM11_CH1	TIM19_CH1	SPI1_SCK/I2S1_CK	-	-	-	-	ESMC_CS2_NCS	-	-	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TIM13_CH1	TIM8_BKIN	SPI1_MISO	TIM1_BKIN		COMP1_OUT	-	ESMC_BK1_IO3	-	LPUART1_CTS	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TIM10_CH1	TIM8_CH1N	SPI1_MOSI/I2S1_SD	TIM1_CH1N	-	COMP2_OUT	-	ESMC_BK1_IO2	-	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	-	EVENTOUT
PA8	MCO	TIM14_CH1	I2C3_SCL	TIM18_CH1	I2C2_SDA	I2S2_MCK	TIM1_CH1	USART1_CK		-	TIM4_ETR				USB1_OTG_FS_SOF	EVENTOUT
PA9	-	-	I2C3_SMBA	TIM18_ETR	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX		TIM15_BKIN	TIM2_CH3	-	-	LCDC_CS1		EVENTOUT
PA10	-	TIM17_BKIN	-	CTC_SYNC	I2C2_SMBA	SPI2_MISO	TIM1_CH3	USART1_RX		-	TIM2_CH4	TIM8_BKIN		LCDC_CS2	USB1_OTG_FS_ID	EVENTOUT
PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	COMP1_OUT	FDCAN1_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2		USB1_OTG_FS_DM	EVENTOUT
PA12	-	TIM16_CH1	-	-	TIM8_CH4		TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	FDCAN1_TX	TIM4_CH2	TIM1_ETR	-		USB1_OTG_FS_DP	EVENTOUT
PA13	SWDIO_JTMS	TIM16_CH1N	-	I2C4_SCL	I2C1_SCL	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	LCDC_RS	-		-	EVENTOUT
PA14	SWCLK_JTCK	LPTIM1_OUT	-	I2C4_SMBA	I2C1_SDA	TIM8_CH2	TIM1_BKIN	USART2_TX	TIM18_CH2	-	-	LCDC_8RD_6RW	-		-	EVENTOUT
PA15	JTDI	TIM2_CH1	TIM8_CH1	TIM18_ETR	I2C1_SCL	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_RX		TIM1_BKIN	-	LCDC_8WR_6E	TIM11_CH1	TIM19_CH1	TIM2_ETR	EVENTOUT

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	TIM3_CH3	TIM18_ETR	TIM8_CH2N	-	TIM1_CH2N	-	-	-	ESMC_BK1_IO1	-	-	ETH_MII_RXD2	-	EVENTOUT
PB1	-	-	TIM3_CH4	TIM9_CH1	TIM8_CH3N	-	TIM1_CH3N	-	COMP4_OUT	-	ESMC_BK1_IO0	-	LPUART1_RTS_DE	ETH_MII_RXD3	-	EVENTOUT
PB2	-	LPTIM1_OUT	TIM5_CH1	TIM18_CH1	I2C3_SMBA	-	-	-	-	-	ESMC_BK2_IO1	-		-	-	EVENTOUT
PB3	JTDO_TRACESWO	TIM2_CH2	TIM4_ETR	TIM18_CH3	TIM8_CH1N	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	USART2_TX	CTC_SYNC	-	TIM3_ETR	-	LCDC_D1	-	-	EVENTOUT
PB4	JTRST	TIM16_CH1	TIM3_CH1	TIM13_CH1	TIM8_CH2N	SPI1_MISO	SPI3_MISO	USART2_RX	-	-	TIM17_BKIN	-	LCDC_D2	-	-	EVENTOUT
PB5	-	TIM16_BKIN	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	USART2_CK	I2C3_SDA	FDCAN2_RX	TIM17_CH1	LPTIM1_IN1	LCDC_D3	ETH_PPS_OUT	USB2_OTG_FS_SOF	EVENTOUT
PB6	-	TIM16_CH1N	TIM4_CH1	TIM10_CH1	-	TIM8_CH1	TIM8_ETR	USART1_TX	COMP4_OUT	FDCAN2_TX	TIM8_BKIN2	LPTIM1_ETR	LCDC_D4	-	-	EVENTOUT
PB7	-	TIM17_CH1N	TIM4_CH2	I2C4_SDA	I2C1_SDA	TIM8_BKIN	-	USART1_RX	COMP3_OUT	-	TIM3_CH4	LPTIM1_IN2	LCDC_D5	-	-	EVENTOUT
PB8	-	TIM16_CH1	TIM4_CH3	-	I2C1_SCL	-	LCDC_D6	USART3_RX	COMP1_OUT	FDCAN1_RX	TIM8_CH2	SDIO_D4	TIM1_BKIN	ETH_MII_TXD3	-	EVENTOUT
PB9	-	TIM17_CH1	TIM4_CH4	TIM14_CH1	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	FDCAN1_TX	TIM8_CH3	SDIO_D5	TIM1_CH3N	LCDC_D7	-	EVENTOUT
PB10	-	TIM2_CH3	-		-	-	-	USART3_TX	LPUART1_RX	-	ESMC_CLK	-	TIM1_BKIN	ETH_MII_RX_ER	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	-	-	-	USART3_RX	LPUART1_TX	-	ESMC_CS0_NCS	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	EVENTOUT
PB12	-	-	TIM5_ETR	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	LPUART1_RTS_DE	FDCAN2_RX	-	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	-	EVENTOUT
PB13	-	-	-	-	-	SPI2_SCK/I2S2_CK	TIM1_CH1N	USART3_CTS	LPUART1_CTS	FDCAN2_TX	-	-	-	ETH_MII_TXD1/ETH_RMII_TXD1	-	EVENTOUT
PB14	-	TIM15_CH1	-	-	-	SPI2_MISO	TIM1_CH2N	USART3_RTS_DE	COMP4_OUT	-	-	-	-	-		EVENTOUT
PB15	-	TIM15_CH2	TIM15_CH1N	COMP3_OUT	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT

3.3. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-5 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	LPTIM1_IN1	TIM1_CH1	-	-	-	-	-	LPUART1_RX	-	ESMC_DQS	-		-	USB2_OTG_FS_DM	EVENTOUT
PC1	-	LPTIM1_OUT	TIM1_CH2	-	-	-	-	-	LPUART1_TX	-	ESMC_BK2_IO0	-	-	ETH_MDC	USB2_OTG_FS_DP	EVENTOUT
PC2	-	LPTIM1_IN2	TIM1_CH3	COMP3_OUT	-	-	-	-	-	-	ESMC_BK2_IO1	-	-	ETH_MII_TXD2	USB2_OTG_FS_ID	EVENTOUT
PC3	-	LPTIM1_ETR	TIM1_CH4	-	I2C2_SCL	-	TIM1_BKIN2	-	-	-	ESMC_BK2_IO2	-	-	ETH_MII_TX_CLK	-	EVENTOUT
PC4	-	-	TIM1_ETR	-	-	-	-	USART1_TX	-	-	ESMC_BK2_IO3	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	-	EVENTOUT
PC5	-	-	TIM15_BKIN		-	-	TIM1_CH4N	USART1_RX	-	-	ESMC_CS1_NCS	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	-	EVENTOUT
PC6	-	-	TIM3_CH1	TIM13_CH1	TIM8_CH1	-	I2S2_MCK	-	I2C4_SCL	-	ESMC_CS3_NCS	SDIO_D6	-	-	-	EVENTOUT
PC7	-	-	TIM3_CH2	TIM10_CH1	TIM8_CH2	-	I2S3_MCK	-	I2C4_SDA	-	-	SDIO_D7	-	-	-	EVENTOUT
PC8	-	-	TIM3_CH3	TIM18_CH1	TIM8_CH3	-	-	-	I2C3_SCL	-	-	SDIO_D0	-	-	-	EVENTOUT
PC9	-	-	TIM3_CH4	-	TIM8_CH4	-	TIM8_BKIN2	-	I2C3_SDA	-	-	SDIO_D1	LCDC_CS3	-	-	EVENTOUT
PC10	-	-	-	-	TIM8_CH1N	UART1_TX	SPI3_SCK/I2S3_CK	USART3_TX	-	-	ESMC_CS4_NCS	SDIO_D2	LCDC_CS0	-	-	EVENTOUT
PC11	-	-	-	-	TIM8_CH2N	UART1_RX	SPI3_MISO	USART3_RX	I2C3_SDA	-	-	SDIO_D3	LCDC_D0	-	-	EVENTOUT
PC12	-	TIM5_CH2	TIM9_CH2	TIM18_CH2	TIM8_CH3N	UART2_TX	SPI3_MOSI/I2S3_SD	USART3_CK	-	-	-	SDIO_CK	-	-	-	EVENTOUT
PC13	-	-	TIM1_BKIN	-	TIM1_CH1N	-	TIM8_CH4N	-	-	-	-	-		-	-	EVENTOUT
PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

3.4. Alternate functions selected through GPIOD_AFR registers for port D

Table 3-6 Port D alternate function mapping

PortD	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	-	-	-	-	-	TIM8_CH4N	-	-	FDCAN1_RX	-	-	LCDC_D2	-	-	EVENTOUT
PD1	-	-	-	-	TIM8_CH4	-	TIM8_BKIN2	-	-	FDCAN1_TX	-	-	LCDC_D3	-	-	EVENTOUT
PD2	-	-	TIM3_ETR	-	TIM8_BKIN	UART2_RX	-	-		-	ESMC_CS5_NCS	SDIO_CMD	-	-	-	EVENTOUT
PD3	-	-	TIM2_CH1/ TIM2_ETR	-	-	-	-	USART2_CTS	-	-	ESMC_CS1_NCS	-		-	-	EVENTOUT
PD4	-	-	TIM2_CH2	-	-	-	-	USART2_RTS_DE	-	-	ESMC_BK2_IO0	-	LCDC_8RD_6RW	-	-	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	ESMC_BK2_IO1	-	LCDC_8WR_6E	-	-	EVENTOUT
PD6	-	-	TIM2_CH4		-	-	-	USART2_RX	-	-	ESMC_BK2_IO2	-	LCDC_CS1	-	-	EVENTOUT
PD7	-	-	TIM2_CH3	-	-	-	-	USART2_CK	-	-	ESMC_BK2_IO3	-	LCDC_CS0	-	-	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	LCDC_D13	ETH_RMII_CRS_DV	-	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	LCDC_D14	ETH_MII_RXD0/ETH_ RMII_RXD0	-	EVENTOUT
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	LCDC_D15	ETH_MII_RXD1/ETH_ RMII_RXD1	-	EVENTOUT
PD11	-	TIM5_ETR	-	-	I2C4_SMBA	-	-	USART3_CTS	-	-	-	-	LCDC_D16	ETH_MII_RXD2	-	EVENTOUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS_DE	-	-	-	-	LCDC_D17	ETH_MII_RXD3	-	EVENTOUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	TIM18_CH2		-	-	-	-	-	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	LCDC_D0	-	-	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	SPI2_NSS/I2S2_W S	-	-	-	-	-	LCDC_D1	-	-	EVENTOUT

3.5. Alternate functions selected through GPIOA_AFR registers for port E

Table 3-7 Port E alternate function mapping

PortE	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	TIM4_ETR	-	TIM16_CH1	-	-	USART1_TX	-	FDCAN1_RX	-	-		-	-	EVENTOUT
PE1	-	-	-	TIM14_CH1	TIM17_CH1	-	-	USART1_RX	-	FDCAN1_TX	-	-		-	-	EVENTOUT
PE2	TRACECK	-	TIM3_CH1	-	-	-	-	-	-	FDCAN2_RX	-	-			-	EVENTOUT
PE3	TRACED0	-	TIM3_CH2	TIM10_CH1	-	-	-	-	-	FDCAN2_TX	-	-			-	EVENTOUT
PE4	TRACED1	-	TIM3_CH3	TIM9_CH1	-	-	-	-	-	-	-	-	LCDC_CS2		-	EVENTOUT
PE5	TRACED2	-	TIM3_CH4	TIM9_CH2	-	-	-	-	-	-	-	-	LCDC_CS3		-	EVENTOUT
PE6	TRACED3	-	-	TIM18_CH4	-	-	-	-	-	-	-	-			-	EVENTOUT
PE7	-	-	TIM1_ETR	TIM18_CH3	-	-	-	-	-	-	-	-	LCDC_D4		-	EVENTOUT
PE8	-	TIM5_CH3	TIM1_CH1N	TIM12_CH1	-	-	-	-	-	-	-	-	LCDC_D5		-	EVENTOUT
PE9	-	TIM5_CH4	TIM1_CH1	TIM12_CH2	-	-	-	-	-	-	ESMC_BK1_IO3	-	LCDC_D6		-	EVENTOUT
PE10	-	-	TIM1_CH2N	TIM18_CH4	-	-	-	-	-	-	ESMC_CLK	-	LCDC_D7		-	EVENTOUT
PE11	-	-	TIM1_CH2	-	-	-	-	-	-	-	ESMC_CS0_NCS	-	LCDC_D8		-	EVENTOUT
PE12	-	-	TIM1_CH3N	-	-	-	-	-	-	-	ESMC_BK1_IO0	-	LCDC_D9	-	-	EVENTOUT
PE13	-	-	TIM1_CH3	-	-	-	-	-	-	-	ESMC_BK1_IO1	-	LCDC_D10	-	-	EVENTOUT
PE14	-	-	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	ESMC_BK1_IO2	-	LCDC_D11	-	-	EVENTOUT
PE15	-	-	TIM1_BKIN	-	-	-	TIM1_CH4N	USART3_RX	-	ESMC_BK1_IO0	ESMC_BK1_IO3	-	LCDC_D12	-	-	EVENTOUT

3.6. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-8 Port F alternate function mapping

PortF	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	EVENTOUT
PF1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	EVENTOUT
PF2	-	-		-	I2C2_SMBA	-	-	-	-	-	-	-		-	-	EVENTOUT
PF3	-	-		TIM15_CH1	-	SPI2_SCK/I2S2_CK	TIM5_CH4	TIM12_CH2	-	-	ESMC_BK1_IO1	-			-	EVENTOUT
PF4	-	-		TIM15_CH2	-	SPI2_SCK/I2S2_CK	-	-	-	-	ESMC_CLK	-	LCDC_RS		-	EVENTOUT
PF5	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

4. Memory mapping

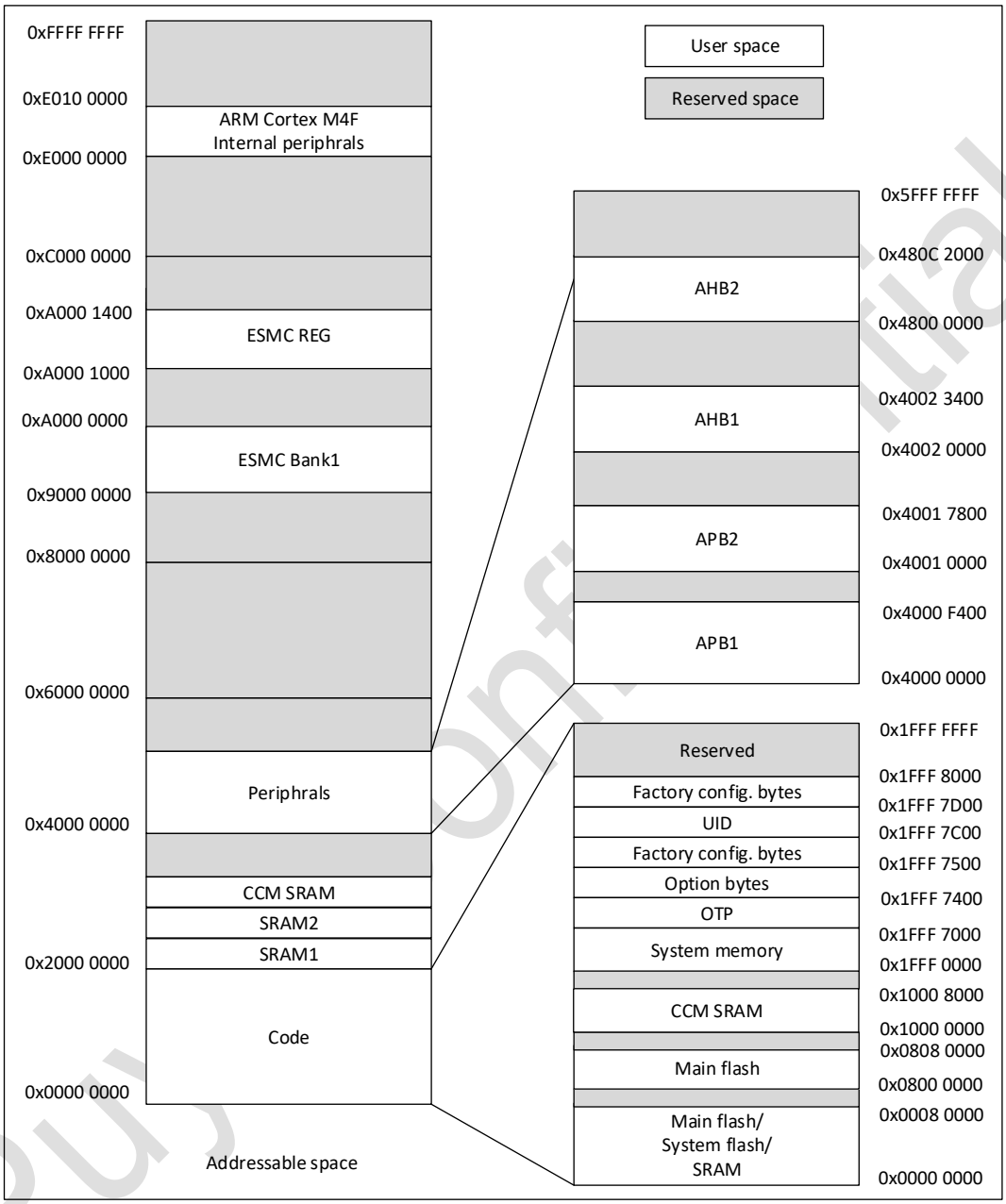


Figure 4-1 Memory mapping

Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2002 4000 - 0x3FFF FFFF	511 MB	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA access.
	0x2000 0000 - 0x2002 3FFF	144 KB	SRAM	If the hardware power-on configuration SRAM is 144 KB, the SRAM address space is 0x2000 0000 - 0x20023FFF
Code	0x1FFF 8000 - 0x1FFF FFFF	32 KB	Reserved	-
	0x1FFF 7E00 - 0x1FFF 7FFF	512 Bytes	UID bytes	Unique ID
	0x1FFF 7C00 - 0x1FFF 7DFF	512 Bytes	Factory config. bytes	-
	0x1FFF 7A00 - 0x1FFF 7BFF	512 Bytes	HSI16 Trim	-
	0x1FFF 7800 - 0x1FFF 79FF	512 Bytes	Factory config. bytes	-
	0x1FFF 7600 - 0x1FFF 77FF	512 Bytes	Factory config. bytes	-
	0x1FFF 7400 - 0x1FFF 75FF	512 Bytes	Option bytes	Option bytes information
	0x1FFF 7000 - 0x1FFF 73FF	1 KB	OTP	-
	0x1FFF 0000 - 0x1FFF 6FFF	28 KB	System memory	Store Bootloader
	0x1008 0000 - 0x1FFE FFFF	256 MB	Reserved	-
	0x1000 0000 - 0x1000 7FFF	32 KB	CCM SRAM	-
	0x0808 0000 - 0x0FFF FFFF	127 MB	Reserved	-
	0x0800 0000 - 0x0807 FFFF	512 KB	Main flash memory	-
	0x0008 0000 - 0x07FF FFFF	127 MB	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA access.
	0x0000 0000 - 0x0007 FFFF	512 KB	Depending on the Boot configuration selection: 1)Main flash memory 2)System memory 3)SRAM	-

1. The address is marked as **Reserved**, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Bus	Memory boundary address	Peripherals
AHB3	0xA000 1000 - 0xA000 13FF	ESMC
AHB2	0x480C 2000 - 0x5FFF FFFF	Reserved
	0x480C 0000 - 0x400C 1FFF	ETH
	0x4808 0000 - 0x480B FFFF	USB2 OTG FS
	0x4804 0000 - 0x4807 FFFF	USB1 OTG FS
	0x4800 2800 - 0x4803 FFFF	Reserved
	0x4800 2400 - 0x4800 27FF	AES
	0x4800 2000 - 0x4800 23FF	SDIO

Bus	Memory boundary address	Peripherals
	0x4800 1800 - 0x4800 1FFF	Reserved
	0x4800 1400 - 0x4800 17FF	GPIOF
	0x4800 1000 - 0x4800 13FF	GPIOE
	0x4800 0C00 - 0x4800 0FFF	GPIOD
	0x4800 0800 - 0x4800 0BFF	GPIOC
	0x4800 0400 - 0x4800 07FF	GPIOB
	0x4800 0000 - 0x4800 03FF	GPIOA
AHB1	0x4002 3400 - 0x4002 FFFF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2400 - 0x4002 2FFF	Reserved
	0x4002 2000 - 0x4002 23FF	FMC
	0x4002 1400 - 0x4002 1FFF	Reserved
	0x4002 1000 - 0x4002 13FF	RCC
	0x4002 0C00 - 0x4002 0FFF	CORDIC
	0x4002 0800 - 0x4002 0BFF	Reserved
	0x4002 0400 - 0x4002 07FF	DMA2
	0x4002 0000 - 0x4002 03FF	DMA1
APB2	0x4001 7800 - 0x4001 FFFF	Reserved
	0x4001 7400 - 0x4001 77FF	LCDC
	0x4001 7000 - 0x4001 73FF	OPA
	0x4001 6C00 - 0x4001 6FFF	COMP
	0x4001 6800 - 0x4001 6BFF	RNG
	0x4001 6400 - 0x4001 67FF	TIMER19
	0x4001 6000 - 0x4001 63FF	TIMER17
	0x4001 5C00 - 0x4001 5FFF	TIMER16
	0x4001 5800 - 0x4001 5BFF	TIMER15
	0x4001 5400 - 0x4001 57FF	TIMER11
	0x4001 5000 - 0x4001 53FF	TIMER10
	0x4001 4C00 - 0x4001 4FFF	TIMER9
	0x4001 4000 - 0x4001 4BFF	Reserved
	0x4001 3C00 - 0x4001 3FFF	ADC3
	0x4001 3800 - 0x4001 3BFF	USART1
	0x4001 3400 - 0x4001 37FF	TIMER8
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	TIMER1
	0x4001 2800 - 0x4001 2BFF	ADC2
	0x4001 2400 - 0x4001 27FF	ADC1
	0x4001 0800 - 0x4001 23FF	Reserved
	0x4001 0400 - 0x4001 07FF	EXTI
	0x4001 0000 - 0x4001 03FF	SYSCFG
APB1	0x4000 F400 - 0x4000 FFFF	Reserved
	0x4000 E000 - 0x4000 F3FF	CAN2.0
	0x4000 CC00 - 0x4000 DFFF	CANFD

Bus	Memory boundary address	Peripherals
	0x4000 C800 - 0x4000 CBFF	CTC
	0x4000 B400 - 0x4000 C7FF	Reserved
	0x4000 AC00 - 0x4000 B3FF	CANMEM
	0x4000 8800 - 0x4000 ABFF	Reserved
	0x4000 8400 - 0x4000 87FF	I2C4
	0x4000 8000 - 0x4000 83FF	LPUART1
	0x4000 7C00 - 0x4000 7FFF	LPTIM1
	0x4000 7800 - 0x4000 7BFF	I2C3
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6D00 - 0x4000 6FFF	Reserved
	0x4000 6C00 - 0x4000 6CFF	BKP
	0x4000 6000 - 0x4000 6BFF	Reserved
	0x4000 5C00 - 0x4000 5FFF	UART3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART2
	0x4000 4C00 - 0x4000 4FFF	UART1
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	Reserved
	0x4000 3C00 - 0x4000 3FFF	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC
	0x4000 2400 - 0x4000 27FF	TIMER18
	0x4000 2000 - 0x4000 23FF	TIMER14
	0x4000 1C00 - 0x4000 1FFF	TIMER13
	0x4000 1800 - 0x4000 1BFF	TIMER12
	0x4000 1400 - 0x4000 17FF	TIMER7
	0x4000 1000 - 0x4000 13FF	TIMER6
	0x4000 0C00 - 0x4000 0FFF	TIMER5
	0x4000 0800 - 0x4000 0BFF	TIMER4
	0x4000 0400 - 0x4000 07FF	TIMER3
	0x4000 0000 - 0x4000 03FF	TIMER2

1. In the above table, the reserved address cannot be written, read back is 0, and a hardfault is generated.

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization,the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 σ).

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C,V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated (mean ±2 σ).

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}-V_{SS}	External supply voltage (including V_{CC}, V_{CCA}, V_{BAT}, V_{REF+}) (1)	-0.3	4.0	V
V_{IN}(2)	FT_xx, NRST I/O input voltage	V_{SS}-0.3	5.5	
	TT_xx I/O input voltage	V_{SS}-0.3	4.0	
$\|\Delta V_{CCx}\|$	Voltage variation between different V_{CC} pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Voltage variation between different ground pins	-	50	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. Maximum V_{IN} must always follow allowable maximum injection current limits as per the table.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC}/V_{CCA} power lines (source)(1)	170	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink) (1)	170	

Symbol	Descriptions	Max	Unit
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	120	
	Total output current sourced by sum of all I/Os and control pins	120	
I_{IO}(2)	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/Os and control pin(3)	30	
$I_{INJ(PIN)}$	Injected current on five-volt tolerant I/O(4)	-5/+0	
	Injected current on any other pin(5)	± 5	
$\Sigma I_{INJ(PIN)}$(7)	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.
3. PC13, PC14, PC15 pins are not included because they are powered by power switch. The current sourced capacity is limited to 3 mA.
4. Negative injection disturbs the analog performance of the device.
5. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
6. A positive injection is induced by $V_{IN} > V_{CCA}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
7. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 5-3 Thermal characteristics

Symbol	Descriptions	Max	Unit
T_{STG}	Storage temperature range	-65 to 150	℃
T_J	Maximum junction temperature	150	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	-	0	170	MHz
f_{PCLK1}	APB1 clock frequency	-	0	85	
f_{PCLK2}	APB2 clock frequency	-	0	85	
V_{CC}	Operating voltage	-	2.3	3.6	V
V_{CCA}	Operating voltage of analog circuit	Must be the same potential as V_{CC}	2.3	3.6	V
V_{BAT}	Backup operating voltage	-	2.3	3.6	V
V_{IN}	FT_xx, NRST I/O input voltage	-	V_{SS}-0.3	5.5	V
	TT_xx I/O input voltage	-	V_{SS}-0.3	3.6	
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	110	℃

5.3.2. Reset and power control block characteristics

Table 5-5 Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	PVD threshold	PLS[2:0]=000 (Rising edge)	Reserved			V
		PLS[2:0]=000 (Falling edge)				

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PLS[2:0]=001 (Rising edge)				
		PLS[2:0]=001 (Falling edge)				
		PLS[2:0]=010 (Rising edge)				
		PLS[2:0]=010 (Falling edge)				
		PLS[2:0]=011 (Rising edge)	2.3(2)	2.4	2.5	
		PLS[2:0]=011 (Falling edge)	2.2	2.3	2.4(2)	
		PLS[2:0]=100 (Rising edge)	2.5(2)	2.6	2.7	
		PLS[2:0]=100 (Falling edge)	2.4	2.5	2.6(2)	
		PLS[2:0]=101 (Rising edge)	2.7(2)	2.8	2.9	
		PLS[2:0]=101 (Falling edge)	2.6	2.7	2.8(2)	
		PLS[2:0]=110 (Rising edge)	2.9(2)	3	3.1	
		PLS[2:0]=110 (Falling edge)	2.8	2.9	3(2)	
		PLS[2:0]=111 (detect PB7 voltage without hysteresis)	-	1.2(2)	-	
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.53	1.63	1.73	V
		Rising edge	1.56	1.61	1.66	
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	20	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1	2.5	4.5	ms

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. The reset temporization is measured from the power-on (POR reset or wake-up from V_{BAT}) to the instant when the first instruction is read by the user application code.

5.3.3. Operating conditions at power-on / power-down

Table 5-6 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	0	∞	μs/V
	V_{CC} fall rate	V_{CC} and V_{BAT} drop synchronously	20	∞	
		V_{CC} drops and V_{BAT} holds	100	∞	

5.3.4. Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. All the run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{CC} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 25 MHz, 1 wait state from 25 to 50 MHz, 3 wait states from 50 to 75 MHz, 4 wait states from 75 to 100 MHz, 5 wait states from 100 to 125 MHz, 6 wait states from 125 to 150 MHz,and 7 wait states beyond 150 MHz).
- The maximum values are obtained for V_{CC} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for $_{TA=}$ 25 °C and V_{CC} = 3.3 V unless otherwise specified.
- Command prefetch function is turned on. When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$.

Note: The command prefetch function must be set before setting the clock and bus frequency divi sion.

Table 5-7 Current consumption in Run mode, processing running from Flash

Symbol	Parameter	Conditions			f_{HCLK}(2)(3)	Typ	Max(1)		Unit
		Code	Run	-		T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{VCC}	Supply current in Run mode	While(1)	Flash	external clock. All peripheral clocks enabled	170 MHz	47.7	-	52.6	mA
					144 MHz	42.8	-	50.3	
					128 MHz	38.7	-	46.8	
					96 MHz	30.0	-	38.6	
					64 MHz	21.2	-	30.4	
					48 MHz	17.8	-	27.3	
					32 MHz	12.8	-	22.7	
					16 MHz	5.5	-	15.9	
				external clock. All peripheral clock disabled	170 MHz	23.2	-	31.8	
					144 MHz	21.6	-	29.2	
					128 MHz	18.6	-	27.9	
					96 MHz	14.8	-	24.1	
					64 MHz	10.8	-	20.6	
					48 MHz	10.0	-	19.8	
					32 MHz	7.5	-	17.4	
					16 MHz	3.4	-	13.3	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.
3. 16 MHz is the internal HSI clock.

Table 5-8 Current consumption in Run mode (SRAM)

Symbol	Parameter	Conditions			f_{HCLK}(2)(3)	Typ	Max(1)		Unit
		Code	Run	-		T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{VCC}	Supply current in Run mode	While(1)	SRAM SRAM1	external clock. All peripheral clocks enabled	170 MHz	47.6	-	48.9	mA
					144 MHz	40.8	-	44.9	
					128 MHz	36.6	-	42.2	
					96 MHz	28.1	-	33.4	
					64 MHz	19.4	-	25.8	
					48 MHz	15.1	-	22.0	
					32 MHz	10.8	-	18.2	
					16 MHz	5.7	-	13.9	
				external clock. All peripheral clock disabled	170 MHz	23.3	-	31.0	
					144 MHz	19.5	-	27.3	
					128 MHz	17.5	-	26.5	
					96 MHz	13.6	-	21.6	
					64 MHz	9.6	-	17.8	
					48 MHz	7.8	-	15.9	
					32 MHz	5.7	-	14.0	
					16 MHz	3.3	-	11.8	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.
3. 16 MHz is the internal HSI clock.

Table 5-9 Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}(2)(3)	Typ	Max(1)		Unit
		Code	-		T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in Sleep mode	While(1)	external clock. All peripheral clocks enabled	170 MHz	37.2	-	45.0	mA
				144 MHz	31.9	-	40.2	
				128 MHz	28.6	-	37.2	
				96 MHz	22.0	-	31.1	
				64 MHz	15.3	-	25.0	
				48 MHz	12.0	-	21.9	
				32 MHz	8.7	-	18.8	
				16 MHz	4.6	-	15.1	
			external clock. All peripheral clock disabled	170 MHz	9.3	-	16.8	
				144 MHz	8.0	-	15.8	
				128 MHz	7.3	-	15.2	
				96 MHz	5.8	-	14.0	
				64 MHz	4.4	-	12.8	
				48 MHz	3.7	-	12.2	
				32 MHz	3.3	-	11.6	
				16 MHz	2.0	-	10.6	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.
3. 16 MHz is the internal HSI clock.

Table 5-10 Current consumptionn in Low power run mode,processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}(2)	Typ	Max(1)		Unit
		Code	-		T_A = 25℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in Lower-power run mode	While(1)	external clock. All peripheral clocks enabled	2 MHz	2.08	-	10.9	mA
				1 MHz	1.71	-	10.7	
				250 kHz	1.42	-	10.5	
				62.5 kHz	1.36	-	10.5	
			external clock. All peripheral clock disabled	2 MHz	1.81	-	10.2	
				1 MHz	1.57	-	10.1	
				250 kHz	1.38	-	10.1	
				62.5 kHz	1.33	-	10.1	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.

Table 5-11 Current consumptionn in Low power run mode,processing running from SARM

Symbol	Parameter	Conditions		f_{HCLK}(2)	Typ	Max(1)		Unit
		Code	-		T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in Lower-power run mode	While(1)	external clock (2). All peripheral clocks enabled	2 MHz	2.29	-	10.5	mA
				1 MHz	2.06	-	10.3	
				250 kHz	1.88	-	10.1	
				62.5 kHz	1.83	-	9.7	
			external clock (2). All peripheral clock disabled	2 MHz	1.93	-	10.0	
				1 MHz	1.85	-	9.9	
				250 kHz	1.78	-	9.8	
				62.5 kHz	1.77	-	9.5	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.

Table 5-12 Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}(2)	Typ	Max(1)		Unit
		Code	-		T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in Low-power Sleep mode	While(1)	external clock (2). All peripheral clocks enabled	2 MHz	1.81	-	11.6	mA
				1 MHz	1.63	-	11.5	
				250 kHz	1.50	-	11.3	
				62.5 kHz	1.47	-	11.3	
			external clock (2). All peripheral clock disabled	2 MHz	1.29	-	9.3	
				1 MHz	1.27	-	9.3	
				250 kHz	1.25	-	9.3	
				62.5 kHz	1.24	-	9.3	

1. Data based on characterization results, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 16 MHz.

Table 5-13 Current consumption in Stop and Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)		Unit
			V_{CC}/V_{BAT} = 2.3 V	V_{CC}/V_{BAT} = 3.3 V	V_{CC}/V_{BAT} = 3.6 V	T_A = 85 °C	T_A = 105 °C	
I_{VCC}	Supply current in Stop mode	In LDO MR (1.1 V) mode, internal high-speed oscillator, internal low-speed oscillator and high-speed oscillator off.	-	1005	-	-	7660	μA
		In LDO LPR (0.9 V) mode, internal high-speed oscillator, internal low-speed oscillator and high-speed oscillator off.	-	499	-	-	7360	
	Supply current in Standby mode	Internal low speed oscillator and IWDG on	-	2.43	-	-	13.1	
		Internal low speed oscillator ON, IWDG off	-	2.40	-	-	13.0	
		Internal low speed RC oscillator and IWDG off, low speed oscillator and RTC off	-	2.08	-	-	12.6	
		SRAM2 is powered in Standby mode	-	5.01	-	-	28.0	
I_{VBAT}	Backup domain supply current	Low speed oscillator and RTC on	-	2.67	-	-	4.23	
		Low speed oscillator and RTC off	-	2.19	-	-	3.92	

1. Typical values are tested at T_A = 25 °C.
2. Evaluated by characterization, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-14 Wake-up time from low-power mode

Symbol	Parameter	Typ[2][3]	Max	Unit
$t_{WUSLEEP}$[1]	Wake-up from Sleep to Run mode	6	-	CPU cycles
$t_{WULPSLEEP}$[1]	Wake-up from Low-power sleep to Low-power run mode	6	-	
t_{WUSTOP}[1]	Wake-up from Stop to Run mode in Flash (LDO MR mode)	6	-	μs
	Wake-up from Stop to Run mode in SRAM (LDO MR mode)	6	-	
	Wake-up from Stop to Run mode in Flash (LDO LPR mode)	8	-	
	Wake-up from Stop to Run mode in SRAM1 (LDO LPR mode)	8	-	
	Wake-up from Stop to Low-power run mode in Flash (LDO LPR mode)	8	-	
	Wake-up from Stop to Low-power run mode in SRAM1 (LDO LPR mode)	8	-	
$t_{WUSTDBY}$[1]	Wake-up from Standby to Run mode	40	-	
$t_{WUSTDBY\_SRAM2}$[1]	Wake-up from Standby to Run mode in SRAM2 ON	40	-	
$t_{WULPRUN}$	Wake-up from Low-power run to Run mode	5	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.
3. Test in HSI16 = 16 MHz.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding I/O is used as a standard GPIO.

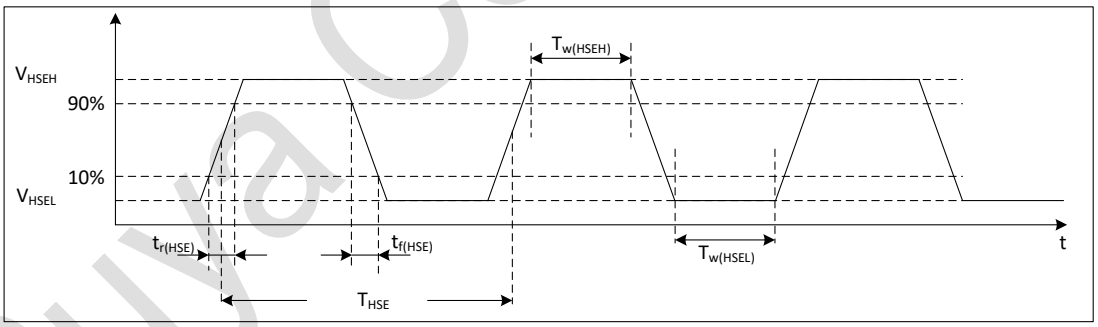


Figure 5-1 High-speed external clock timing diagram

Table 5-15 High-speed external clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	1	-	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3*V_{CC}	
$t_{w(HSE)}$	OSC_IN high or low time		5	-	-	ns
$t_{r(HSE)}$ /$t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input pin capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

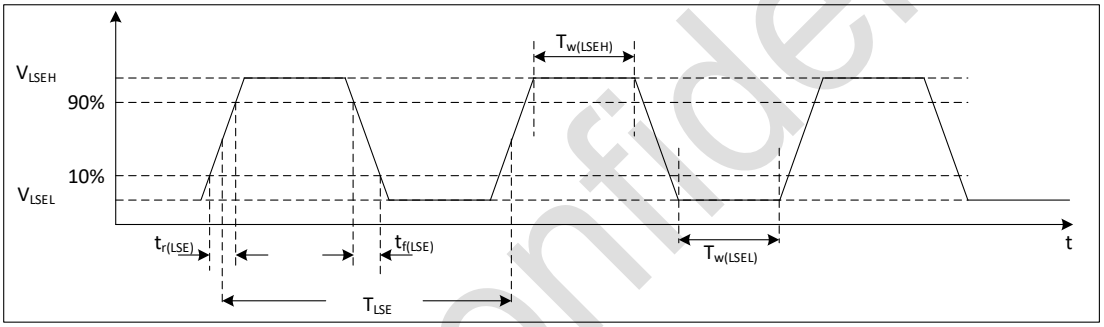


Figure 5-2 Low-speed external clock timing diagram

Table 5-16 Low-speed external clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.7*V_{CC}	-	V_{CC}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3*V_{CC}	
$t_{w(LSE)}$	OSC32_IN high or low time		450	-	-	ns
$t_{r(LSE)}$ /$t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSC32_IN input pin capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	40	-	60	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-17 HSE oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-		4	-	32	MHz
R_F	Feedback resistor	-		-	385	-	kΩ
I_{CC}	HSE current consumption	CL = 11 pF @ 4 MHz, Rm = 100 Ω, HSE_DRV [1: 0] = 00		-	1	-	mA
		CL = 11 pF @ 8 MHz, Rm = 80 Ω, HSE_DRV [1: 0] = 00		-	1	-	
		CL = 11 pF @ 16 MHz, Rm = 30 Ω, HSE_DRV [1: 0] = 01		-	1.2	-	
		C_L=19 pF@24 MHz,Rm=40 Ω,HSE_DRV[1:0]=10		-	1.6	-	
		C_L=9 pF@32 MHz,Rm=40 Ω,HSE_DRV[1:0]=10		-	1.7	-	
g_m	Maximum critical crystal gm	Startup	HSE_DRV[1:0]=00	3.5	-	-	mA/V
			HSE_DRV[1:0]=01	5	-	-	
			HSE_DRV[1:0]=10	7.5	-	-	
			HSE_DRV[1:0]=11	10	-	-	
$t_{SU(HSE)}$(2)	Startup time	HSE_EN to rising edge of first duty cycle stable clock	C_L = 11 pF @ 4 MHz, Rm = 100 Ω, HSE_DRV [1: 0] = 00	-	1.6	-	ms
			C_L = 11 pF @ 8 MHz, Rm = 80 Ω, HSE_DRV [1: 0] = 00	-	0.9	-	
			C_L = 11 pF @ 16 MHz, Rm = 30 Ω, HSE_DRV [1: 0] = 01	-	0.7	-	
			C_L=19 pF@24 MHz, Rm=40 Ω,HSE_DRV[1:0]=10	-	1.3	-	
			C_L=9 pF@32 MHz, Rm=40 Ω,HSE_DRV[1:0]=10	-	1.1	-	

1. Evaluated by characterization, not tested in production.
2. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-18 LSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF	Feedback resistor	-	-	5	-	MΩ
I_{CC}	LSE current consumption	C_L=6 pF,LSE_DRV[1:0]=00	-	600	-	nA
		C_L=6 pF,LSE_DRV[1:0]=01	-	700	-	
		C_L=12 pF,LSE_DRV[1:0]=10	-	1000	-	
		C_L=12 pF,LSE_DRV[1:0]=11	-	1400	-	
g_m	Maximum critical crystal gm	LSE_DRV[1:0]=00	2.5	-	-	μA/V
		LSE_DRV[1:0]=01	3.75	-	-	
		LSE_DRV[1:0]=10	8.5	-	-	
		LSE_DRV[1:0]=11	3.5	-	-	
$t_{SU(LSE)}$(2)	Startup time	C_L=6 pF,LSE_DRV[1:0]=00	-	2.7	-	s
		C_L=6 pF,LSE_DRV[1:0]=01	-	1.3	-	
		C_L=12 pF,LSE_DRV[1:0]=10	-	1.5	-	
		C_L=12 pF,LSE_DRV[1:0]=11	-	0.8	-	

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-19 High-speed internal (HSI 16) RC oscillator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	HSI16 frequency	V_{CC}=3.3 V,T_A = 25 °C		15.92	16	16.08	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
$\Delta V_{CC(HSI)}$	HSI16 frequency drift over temperature	-		-0.8	-	0.8	%
ACC_{HSI}	Accuracy of HSI16 oscillator	Using the RCC_CR register to adjust(1)		-	0.5	1(3)	%
		Factory calibration(2)	T_A = 0 to 85 °C	-2	-	1.5	%
			T_A = -40 to 105 °C	-2.5	-	2	
$t_{su(HSI)}$(2)	HSI16 oscillator startup time	-		-	2.9	-	μs
$I_{CC(HSI)}$(2)	HSI16 oscillator power consumption	16 MHz		-	230	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-20 High-speed internal (HSI 48) RC oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI48 frequency	V_{CC}=3.3 V, T_A = 25 °C	47.64	48	48.34	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ΔTemp(HSI)	HSI 48M frequency drift over temperature	T_A = 0 to 85 °C	-2.5		1.5	%
		T_A = -40 to 105 °C	-3		2	
$t_{su(HSI)}$(2)	HSI48 oscillator startup time	-	-	2.9	-	μs
$I_{CC(HSI)}$(2)	HSI48 oscillator power consumption	48 MHz	-	360	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-21 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{CC} = 3.3 V, T_A = 25 °C	38.6	40	41.4	kHz
		V_{CC} = 2.3 to 3.6 V, T_A = -40 to 105 °C	30	40	50	kHz
$t_{su(LSI)}$(1)	LSI oscillator startup time	-	-	-	85	μs
$I_{CC(LSI)}$(1)	LSI oscillator power consumption	-	-	0.4	-	μA

1. Guaranteed by design, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-22 PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock	2	-	32	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}(2)	PLL multiplier output clock	24	-	170	MHz
t_{LOCK}	PLL lock time	-	25	100	μs
Jitter	Jitter	-	360	-	ps

1. Guaranteed by design, not tested in production.
2. The PLL output frequency (f_{PLL_OUT} < 96 MHz) must first be multiplied to exceed 96 MHz before being divided down to the target frequency.

5.3.10. Memory characteristics

Table 5-23 Memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
PE_{CYC}	Endurance	T_A = -40 to 85 °C	100	-	-	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 55 ℃	30	-	-	years
		1 kcycle at T_A = 85 ℃	15	-	-	
		1 kcycle at T_A = 105 ℃	10	-	-	
		10 kcycle at T_A = 55 ℃	10	-	-	
t_{PROG}	Page programming time	T_A = -40 to 105 °C	-	1.5	-	ms
t_{ERASE}	Page erase time	T_A = -40 to 105 °C	-	5	-	ms
t_{MERASE}	Mass erase time	T_A = -40 to 105 °C	-	5	-	ms

1. Guaranteed by design, not tested in production.

5.3.11. EFT characteristics

Table 5-24EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

5.3.12. ESD & LU characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Table 5-25 ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C,JESD22-A114	-	-	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	T_A = 25 °C,JESD22-C101	-	-	1000	V
LU	Overcurrent test	T_A = 25 °C,JESD78A	-	-	±200	mA
	Overvoltage test		-	-	5.4	V

5.3.13. I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{CC} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

An out of range parameter indicates the failure: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of – 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Table 5-26 I/O current injection susceptibility

Symbol	Descriptions	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injection current on PC13, PC14, PC15 pins	0	0	mA
	Injected current on 5V-tolerant I/O	-5	0	
	Injected current on any other pin	-5	5	

5.3.14. I/O port characteristics

Table 5-27 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TT_xx I/O,1.8 V≤V_{CC}≤ 3.6 V	-0.3	-	0.35 V_{CC}-0.06	V
		FT_xx I/O,1.8 V≤V_{CC}≤ 3.6 V	-0.3	-	0.4 V_{CC}-0.04	
V_{IH}	Input high level voltage	TT_xx I/O,1.8 V≤V_{CC}≤ 3.6 V	0.6 V_{CC}+0.14	-	V_{CC}+0.3	V
		FT_xx I/O,1.8 V≤V_{CC}≤ 3.6 V	0.45 V_{CC}+0.23	-	5.5	
V_{hys}(1)	Schmitt trigger hysteresis	-	-	100	-	mV
V_{lkg}(2)	Input leakage current	TT_xx I/O, V_{SS}≤V_{IN}≤V_{CC}	-	-	-1	μA
		FT_xx I/O, V_{IN} =5 V	-	-	3	
R_{PU}(3)	Internal pull-up resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}(3)	Internal pull-down resistor	V_{IN} = V_{CC}	30	40	50	kΩ
C_{IO}	Pin capacitance	-	-	5	-	pF
$t_{ns(EXTI)}$ (1)	Input filter width	ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$ (1)	I^2C Input filter width	ENI=1, EIIC=1	50	140	250	ns
$t_{ns(NRST)}$(1)	NRST input filter width	ENI=1, EIIC=1	100	180	300	ns

1. Guaranteed by design, not tested in production.
2. If there is reverse current pouring in adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be a real resistor in series with a switchable PMOS/NMOS.

Output driving current

The GPIOs (general-purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH})

PC13、PC14、PC15 in V_{BKP} domain are powered via a current-limited switch (3 mA sourcing).the use of GPIOs PC13 to PC15 in output mode is limited:the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins, which can drive current must be limited to respect the absolute maximum rating.

- The sum of the currents sourced by all the I/Os on V_{CC}, plus the maximum Run consumption of the MCU sourced on V_{CC}, cannot exceed the absolute maximum rating ΣI_{VCC}.in Table 5-2 Current characteristics
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS}.in Table 5-2 Current characteristics

Output voltage

Unless otherwise specified, the parameters given in table below are derived from tests performed under ambient temperature and V_{CC} supply voltage conditions.

Table 5-28 Output voltage characteristics(1)

Symbol	Parameter	Conditions(2)	Min(1)	Typ	Max(1)	Unit
V_{OL}	Output low level voltage	3 V≤V_{CC}≤ 3.6 V,I_{IO} = +20 mA (Up to 6 pins are allowed to sink current simultaneously)	-	-	0.5	V
	Output low level voltage	2.7 V≤V_{CC}≤ 3.6 V,I_{IO} = +8 mA (Up to 8 pins are allowed to sink current simultaneously)	-	-	0.4	
		2.3 V≤V_{CC}≤ 2.7 V,I_{IO} = +4 mA (Up to 8 pins are allowed to sink current simultaneously)	-	-	0.5	
V_{OH}	Output high level voltage	3.3 V≤V_{CC}≤ 3.6 V,I_{IO} = +20 mA (Up to 6 pins are allowed to output current simultaneously)	V_{CC}-0.5	-	-	V
	Output high level voltage	2.7 V≤V_{CC}≤ 3.6 V,I_{IO} = +8 mA (Up to 8 pins are allowed to output current simultaneously)	V_{CC}-0.4	-	-	
		2.3 V≤V_{CC}≤ 2.7 V,I_{IO} = +4 mA (Up to 8 pins are allowed to output current simultaneously)	V_{CC}-0.5	-	-	

1. Data based on characterization results, not tested in production.
2. The test conditions for driving all IOs is that GPIOx_OSPEEDR = 11.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.

5.3.15. ADC characteristics

Table 5-29 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	-	2.3	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.3	-	V_{CCA}	V
I_{CCA}	V_{CCA} pin current	f_{ADC} = 16 MHz	-	2000	2500(1)	μA
		f_{ADC} = 48 MHz	-	2200	2800(1)	
		f_{ADC} = 64 MHz	-	2200	3000(1)	
I_{REF+}	V_{REF+} pin voltage	f_{ADC} = 16 MHz	-	40	50(1)	μA
		f_{ADC} = 48 MHz	-	120	140(1)	
		f_{ADC} = 64 MHz	-	120	150(1)	
f_{ADC}	ADC clock frequency	2.3≤V_{CCA}<3.6V	16	-	16	MHz
		2.4≤V_{CCA}<3.6V	16	-	48	
		3.0≤V_{CCA}<3.6V,	16	-	64	
f_S(2)	Sampling rate	V_{CCA}≥2.3 V	1	-	1	Msps
		V_{CCA}≥2.4 V	1	-	3	
		V_{CCA}≥3.0 V	1	-	4	
V_{AIN}	Conversion voltage range(3)	Single-ended mode	0	-	V_{REF+}	V
		Differential mode	-V_{REF+}	-	V_{REF+}	
R_{AIN}(2)	External Input Impedance(4)	-	-	-	100	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1.2	kΩ
C_{ADC}(2)	Internal sampling and holding capacitor	-	-	2.5	3	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz	12			μs
		-	192			1/f_{ADC}
t_S(2)	Sampling time	f_{ADC} = 16 MHz	0.156	-	40.03	μs
		-	2.5	-	640.5	1/f_{ADC}
t_{samp_setup}	Sampling time for internal channels	-	20	-	-	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{STAB}(2)	Power-on Stabilization time	-	0	0	3	μs
t_{CONV}(2)	Total conversion time	f_{ADC} = 16 MHz	1	-	40.875	μs
		-	16 to 654			1/f_{ADC}

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. For some package types, V_{REF+} can be internally connected to V_{CCA}, and V_{REF-} can be internally connected to V_{SSA}. For details, please refer to the pin definitions.
4. When using external triggering, an additional delay of 1/f_{PCLK2} is required.
   a) $R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$
   b) The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 5-30 R_{AIN}- max for f_{ADC} = 64 MHz(1)

Sampling period (T_S)	Sampling time (t_s)	Maximum value of R_{AIN} (Ω)	
		Fast channel	Slow channel
2.5	39.06	100	N/A
6.5	101.56	330	100
12.5	195.31	680	470
24.5	382.81	1500	1200
47.5	742.19	2200	1800
92.5	1445.31	4700	3900
247.5	3867.19	12000	10000
640.5	10007.81	39000	33000

1. Guaranteed by design, not tested in production.

Table 5-31 ADC static characteristics (1)(2)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	2.3V≤V_{CCA}=V_{REF+}≤3.6V:1 Msps 2.4V≤V_{CCA}=V_{REF+}≤3.6V:3 Msps 3.0V≤V_{CCA}=V_{REF+}≤3.6V:4 Msps Resolution = 12 bit Fast channel: f_S≤4 MSPS	Single-ended mode	-	±4.5	±12	LSB
			Differential mode	-	±3.0	±8.0	
EO	Offset error		Single-ended mode	-	1.6	±6.0	
			Differential mode	-	-1.0	±4.5	
EG	Gain error		Single-ended mode	-	2.0	±9.0	
			Differential mode	-	0	±2.0	
ED	Differential linearity error		Single-ended mode	-	±1.1	±1.3	
			Differential mode	-	±1.0	±1.3	
EL	Integral linearity		Single-ended mode	-	±2.5	±7.0	
			Differential mode	-	±2.5	±5.5	

1. Guaranteed by design, not tested in production.

2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-32 ADC dynamic characteristics(1)(2)(3)

Symbol	Parameter	Parameter conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	2.3 V≤V_{CCA} = V_{REF+}≤3.6 V:1 Msps 2.4 V≤V_{CCA} = V_{REF+}≤3.6 V:3 Msps 3.0 V≤V_{CCA} = V_{REF+}≤3.6 V:4 Msps Resolution = 12 bit Fast channel: f_S ≤ 4 Msps	Single-ended mode	-	10.0	-	bit
			Differential mode	-	10.3	-	
SINAD	Signal to noise and distortion ratio		Single-ended mode	-	62.4	-	dB
			Differential mode	-	63.7	-	
SNR	Signal to noise ratio		Single-ended mode	-	63.5	-	
			Differential mode	-	68.7	-	
SFDR	spurious free dynamic range		Single-ended mode	-	73.5	-	
			Differential mode	-	68.8	-	
THD	Total harmonic distortion		Single-ended mode	-	-70.0	-61.9	
			Differential mode	-	-65.5	-69.8	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

5.3.16. DAC characteristics

Table 5-33 DAC characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	-	2.3	-	3.6	V
V_{REF+}	Positive reference voltage	V_{REF+} ≤ V_{CCA}	2.3	-	3.6	V
V_{SSA}	Ground	-	0	-	0	V
R_{LOAD}(1)	Load connected to V_{SSA}	-	5	-	-	kΩ
	Load connected to V_{CCA}	-	15	-	-	kΩ
R_O(1)	Impedance output with buffer OFF	The minimum resistive load between DAC_VOUT and V_{SS} to have a 1% accuracy is 1.5 MΩ when the buffer is OFF.	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).	-	-	50	pF
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	It gives the maximum output excursion of the DAC Corresponds to 12-bit input codes (0x0E0) through	0.2	-	-	V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON		-	-	V_{CCA}– 0.2	V

Symbol	Parameter	Note	Min	Typ	Max	Unit
		(0xF1C) (at V_{REF}+ = 3.6 V) and (0x164) through (0xE9C) (at V_{REF+} = 2.3 V)				
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	It gives the maximum output excursion of the DAC.	-	0.5	-	mV
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF		-	-	V_{REF+} - 10 mV	V
$I_{CCVREF+}$	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	With no load, worst code (0x0E4) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.	-	-	380	µA
I_{CCA}	DAC DC V_{CCA} current consumption in quiescent mode(2)	With no load, middle code (0x800) on the inputs	-	-	380	µA
		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs	-	-	480	µA
DNL(3)	Differential non linearity (Difference between two consecutive code-1 LSB)	Given for the DAC in 10-bit configuration	-	±2		LSB
		Given for the DAC in 12-bit configuration	-	±2.5		LSB
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	Given for the DAC in 10-bit configuration	-	±2		LSB
		Given for the DAC in 12-bit configuration	-	±2.5		LSB
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	Given for the DAC in 12-bit configuration	-	-	±12	LSB
		Given for the DAC in 10-bit at V_{REF+} = 3.6 V	-	-	±3	LSB
		Given for the DAC in 12-bit at V_{REF+} = 3.6 V	-	-	±12	LSB
Gain error(2)	Gain error	Given for the DAC in 12-bit configuration	-	-	±0.5	%
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	-	3	4	µs
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ input code between lowest and highest possible ones.	-	6.5	10	µs
PSRR+(1)	Power supply rejection ratio (to V_{CCA}) (static DC measurement)	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.

5.3.17. Comparator characteristics

Table 5-34 Comparator characteris (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Comparator supply voltage	-	2.3	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode	-	-	5	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	0.9	2.3	µs
			>200 mV step 100 mV over-drive	-	-	3.4	
V_{offset}	Offset voltage	-		-	±10	-	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	
I_{CCA}	V_{CCA} supply current	High-speed mode	Static	-	450	720	µA
			With 50 kHz and ±100 mv overdrive square signal	-	450	-	
		Medium-speed mode	Static	-	10	20	
			With 50 kHz and ±100 mv overdrive square signal	-	12	-	
I_{sleep}	Sleep power consumption	-	-	-	10	-	nA

1. Guaranteed by design, not tested in production.

5.3.18. Operational amplifier characteristics

Table 5-35 Operational amplifier characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply voltage	-	2.3	3.3	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{CCA}	V
V_{os}	Offset voltage	25 °C, Output no load	-	-	±3	mV
		Full voltage, full temperature	-	-	±5	
I_{LOAD}	Driving current	-	-	-	2.5	mA
I_{LOAD_PGA}	Drive current (PGA mode)	-	-	-	1.5	mA
C_{LOAD}	Load capacitance	-	-	-	50	pF
R_{LOAD}	Load resistor	-	4	-	-	kΩ
C_{MRR}	Common mode rejection ratio	Frequency: 1 kHz	-	60	-	dB
PSRR	Power supply rejection ratio (to V_{CCA}) (static DC measurement)	Frequency 1 kHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, Vcom = V_{CCA}/2	-	80	-	dB
		Frequency 1 MHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, V_{com} = V_{CCA}/2	40	-	-	
		Frequency 10 MHz, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 kΩ, V_{com} = V_{CCA}/2	20	-	-	
GBW	Bandwidth	200 mV ≤ Vout ≤ V_{CCA}-200 mV	5	10	-	MHz
SR	Slew rate (from 10% * V_{CCA} to 90% * V_{CCA})	Normal mode C_L= 8 pF	4	10	-	V/µ s
		Internal mode C_L= 50 pF	2	5	-	
		High-speed mode C_L= 50 pF	3	7	-	
AO	Open loop gain	100 mV ≤ Vout ≤ V_{CCA}-100 mV	65	95	-	dB
		200 mV ≤ Vout ≤ V_{CCA}-300 mV	75	95	-	
V_{OHSAT}	Maximum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at V_{CCA}. follow mode	V_{CCA}-100	-	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OLSAT}	Minimum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at 0. follow mode	-	-	100	mV
Φm	Phase margin	Follow mode, Vcom = V_{CCA}/2	55	65	-	°
GM	Gain margin	Follow mode, Vcom = V_{CCA}/2	8	-	-	dB
t_{SU}	Start up time (off to output 98% * $_{VCCA}$)	Normal mode, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 k Ω, Follow mode	-	3	6	μs
		High-speed mode, C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 4 k Ω, Follow mode	-	3	6	
PGA Gain error	Positive Phase Gain Gain error	PGA Gain = 2 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	%
		PGA gain= 4, 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	
		PGA gain= 8, 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	
		PGA gain= 16, 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-4		4	
		PGA gain = 32, 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-8		8	
	Inverted gain error	PGA Gain = -1 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	%
		PGA Gain = -3 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	
		PGA Gain = -7 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-2	-	2	
		PGA Gain = -15 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-4		4	
		PGA Gain = -31 200 mV ≤ Vout ≤ V_{CCA}-200 mV	-8		8	
Resistor network	R2/R1 (internal resistance ratio (PGA mode, positive phase input))	PGA gain = 2	-	320/320	-	kΩ/ kΩ
		PGA gain = 4	-	480/160	-	
		PGA gain = 8	-	560/80	-	
		PGA gain = 16		600/40		
		PGA gain = 32		620/20		
	R2/R1 (internal resistance ratio (PGA mode, inverting input))	PGA gain = -1	-	320/320	-	kΩ/ kΩ
		PGA gain = -3	-	480/160	-	
		PGA gain = -7	-	560/80	-	
		PGA gain = -15		600/40		
		PGA gain = -31		620/20		
eN	Voltage noise density	1 kHz, output resistive load 4 kΩ	-	250	-	uV/√Hz
		10 kHz, output resistive load 4 kΩ	-	90	-	
I_{CCA}	OPAMP supply current	Normal mode, No load, Follow mode	-	2.3	2.5	mA
		High speed mode, No load, Follow mode	-	2	2.6	
I_{CCA_INT}	OPAMP Operating current, OPAINTOEN=1	Normal mode, No load, Follow mode	-	1.2	1.5	mA
		High speed mode, No load, Follow mode	-	1.3	1.6	

1. Guaranteed by design, not tested in production.

5.3.19. Temperature sensor characteristics

Table 5-36 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
A_{vg_Slope}(1)	Average slope	2.0	2.2	2.4	mV/°C
V_{30}(1)	Voltage at 30 ℃	0.582	0.6	0.618	V
t_{START}(2)	Start up time	4	-	10	μs
t_{S_temp}(2)(3)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.

5.3.20. Embedded voltage reference characteristics

Table 5-37 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	10	-	-	μs
t_{START}	Startup time	-	3	10	μs
T_{Coeff}(1)	Temperature coefficient of V_{REFINT}	-	-	100	ppm/℃

1. Guaranteed by design, not tested in production.

5.3.21. ADC/DAC reference voltage

Table 5-38 ADC/DAC voltage reference buffer(V_{REFBUF}) characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	1.024 V internal reference buffer	2.3	-	3.6	V
		2.048 V internal reference buffer	2.4	-	3.6	
		2.5 V internal reference buffer	2.8	-	3.6	
		2.9 V internal reference buffer	3.2	-	3.6	
V_{REF10}	1.08 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	1.069	1.08	1.091	V
V_{REF20}	2.048 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	2.028	2.048	2.068	
V_{REF25}	2.5 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	2.475	2.50	2.525	
V_{REF29}	2.9 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	2.871	2.90	2.929	
T_{coeff}(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	-	120	ppm/°C
PSRR +	Power Supply Rejection Ratio	-	-	-	-40	dB
I_{load}	Static load current	-	-	-	6.5	mA
C_L	Load capacitance	-	0.5	1	1.5	μF
ESR	equivalent series resistance	-	-	-	2	Ω
t_{START}	Startup time	C_L = 0.5 μF	-	300	350	μs
		C_L = 1 μF	-	500	650	
		C_L = 1.5 μF	-	650	800	
$I_{CCA(VREFBUF)}$	V_{CCA} consumption	-	-	400	-	μA

1. Guaranteed by design, not tested in production.

2. When using 1.024 V, 2.5 V, and 2.9 V, the Trim values corresponding to the different reference voltages are required to be loaded into the specified locations, as described in the reference manual.

5.3.22. COMP voltage reference buffer characteristics

Table 5-39 Internal voltage reference buffer(V_{REFCMP}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog power supply	0.6 V internal reference buffer	2.3		3.6	V
		1.5 V internal reference buffer	2.3		3.6	
		2.048 V internal reference buffer	2.4		3.6	
		2.5 V internal reference buffer	2.8		3.6	
V_{REF6}	0.6 V internal reference buffer	T_A =25 °C,V_{CC}=3.3 V	0.594	0.6	0.606	V
V_{REF15}	1.5 V internal reference buffer	T_A =25 °C,V_{CC}=3.3 V	1.485	1.5	1.515	
V_{REF20}	2.048 V internal reference buffer	T_A =25 °C,V_{CC}=3.3 V	2.028	2.048	2.068	
V_{REF25}	2.5 V internal reference buffer	T_A =25 °C,V_{CC}=3.3 V	2.475	2.5	2.525	
T_{coeff}(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	-	120	ppm/°C
t_{START}	Startup time	-	-	-	10	µs

1. Guaranteed by design, not tested in production.
2. When using 0.6 V, 1.5 V, and 2.5 V, the Trim values corresponding to the different reference voltages are required to be loaded into the specified locations, as described in the reference manual.

5.3.23. Timer characteristics

Table 5-40 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	-	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 170 MHz	-	-	MHz
Res_{TIM}	Timer resolution time	-	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	-	-	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	-	-	s

Table 5-41 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-42 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.24. Communication interfaces

5.3.24.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and reference manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-43 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

The I²C timings requirements are specified by design when the I²C peripheral is properly configured. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not true open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{CC} is disabled, but is still present.

Table 5-44 I²C filter characteristics

Symbol	Parameter	Standard I²C(1)		Fast I²C(1)(2)		Fm+ I²C(1)(2)		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4	-	0.6	-	0.2	-	µs
$t_{su(SDA)}$	SDA setup time	2000	-	800	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	250	-	250	-	130	-	
$t_{r(SDA)}$ /$t_{r(SDL)}$	SDA and SCL rise time	-	1000	-	300	-	120	
$t_{f(SDA)}$ /$t_{f(SDL)}$	SDA and SCL fall time	-	300	-	300	-	120	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.2	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.2	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.2	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
C_b	Capacitive load for each bus line	-	400	-	400	-	400	pF
t_{sp}	Pulse width of the spikes	0	50(3)	0	50(3)	-	50	µs

1. Guaranteed by design, not tested in production.
2. f_{PCLK} must be at least 4 MHz to achieve standard mode I²C frequencies. f_{PCLK} must be at least 8 MHz to achieve fast mode I²C frequencies. f_{PCLK} must be at least 16 MHz to achieve fast mode plus I²C frequencies.

3. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max).

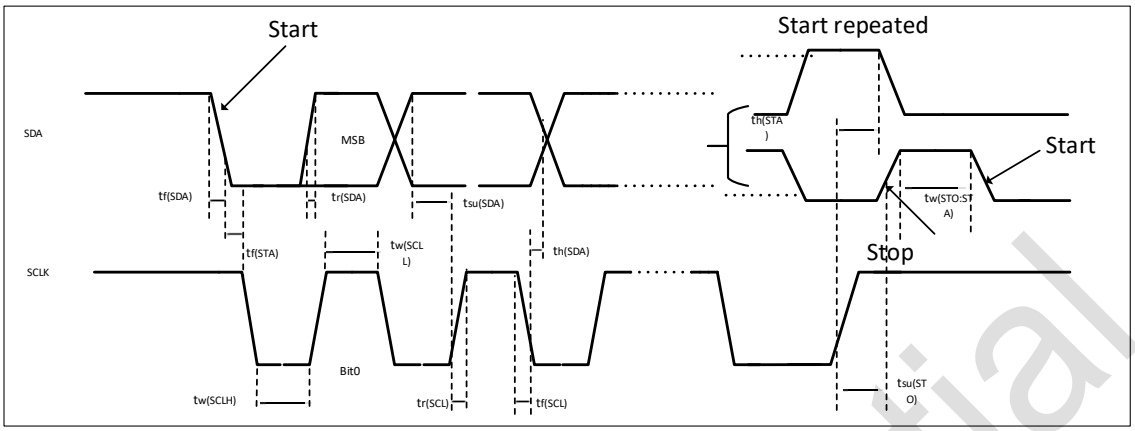


Figure 5-3 I²C bus timing diagram

5.3.24.2. SPI interface characteristics

Table 5-45 SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCK}/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	42.5	MHz
		Slave mode	-	-	42.5	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high level/low level time	Master mode, presc = 2	T_{pclk}-1	T_{pclk}	T_{pclk} +1	
$t_{su(MI)}$	Data input setup time	Master mode	6	-	-	
$t_{su(SI)}$		Slave mode	5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5.5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	
$t_{v(SO)}$	Data output valid time	Slave mode, presc = 2	-	9	12	
$t_{v(MO)}$		Master mode (after enable edge)	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	6(1)	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	-	

1. The Slave updates the data before the transmit edge if the SCK duty cycle sent by the Master is wide between the receive edge and the transmit edge.

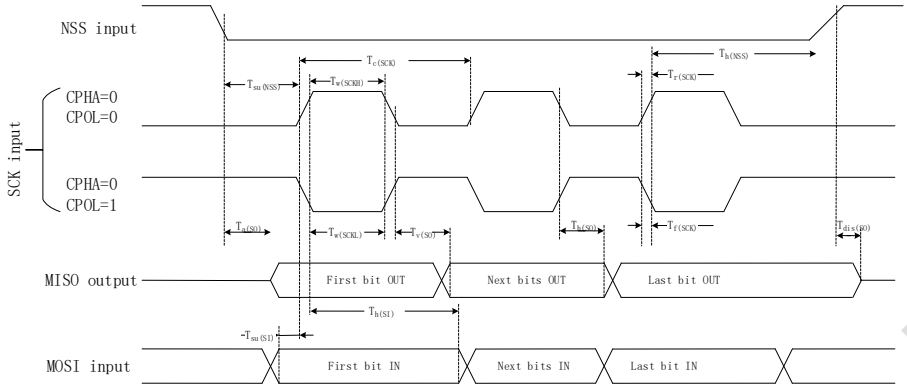


Figure 5-4 SPI timing diagram – slave mode and CPHA=0

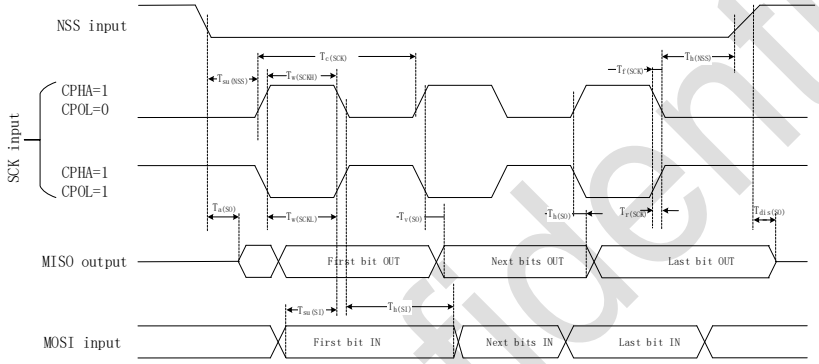


Figure 5-5 SPI timing diagram – slave mode and CPHA = 1(1)

1. Measurement points are set at CMOS level: 0.3 V_{CC} and 0.7 VCC

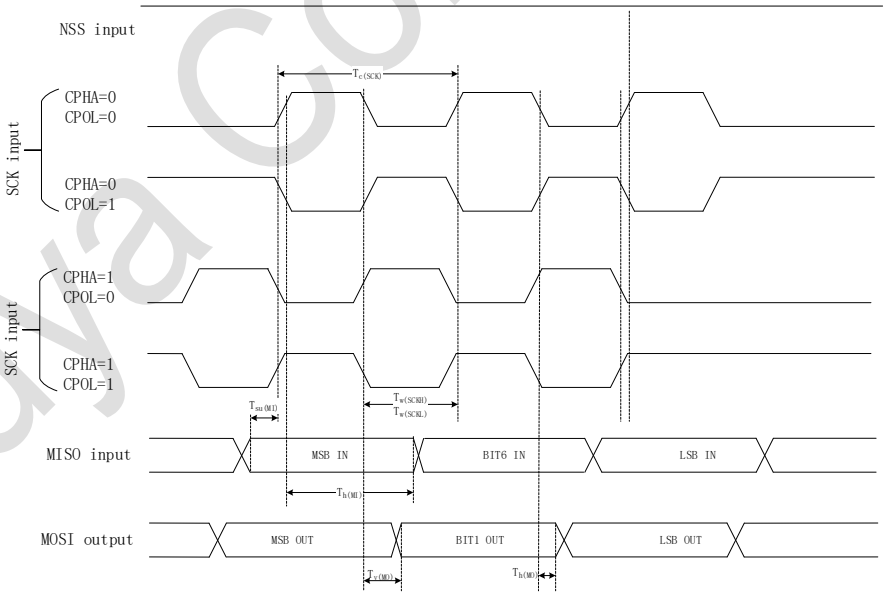


Figure 5-6 SPI timing diagram - slave mode(1)

1. Measurement points are done at CMOS level: 0.3 VCC and 0.7 VCC

5.3.24.3. I²S characteristics

Table 5-46 I²S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_S	I²S sampling frequency	-		8	192	kHz
f_{MCLK}	I²S main clock output	-		0.256 x f_S	0.256 x f_S	MHz
$f_{CK}1/t_{c(CK)}$	I²S clock frequency	Master data		-	64 x f_S	MHz
		Slave master		-	64 x f_S	
D_{CK}	I²S clock frequency duty cycle	Slave receiver		30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$	WS valid time	Master mode		-	2	
$t_{h(WS)}$	WS hold time	Master mode		3	-	
		Slave mode		2	-	
$t_{su(WS)}$	WS setup time	Slave mode		4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver		3	-	
$t_{su(SD\_SR)}$		Slave receiver		4	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver		5	-	
$t_{h(SD\_SR)}$		Slave receiver		2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave receiver (after enable edge)	V_{CC} = 2.7 to 3.6 V	-	15	
			V_{CC} = 2.3 - 3.6 V	-	22	
$t_{v(SD\_MT)}$		Master receiver (after enable edge)		-	2	
$t_{h(SD\_ST)}$	Data output hold time	Slave receiver (after enable edge)		7	-	
$t_{h(SD\_MT)}$		Master receiver (after enable edge)		1	-	

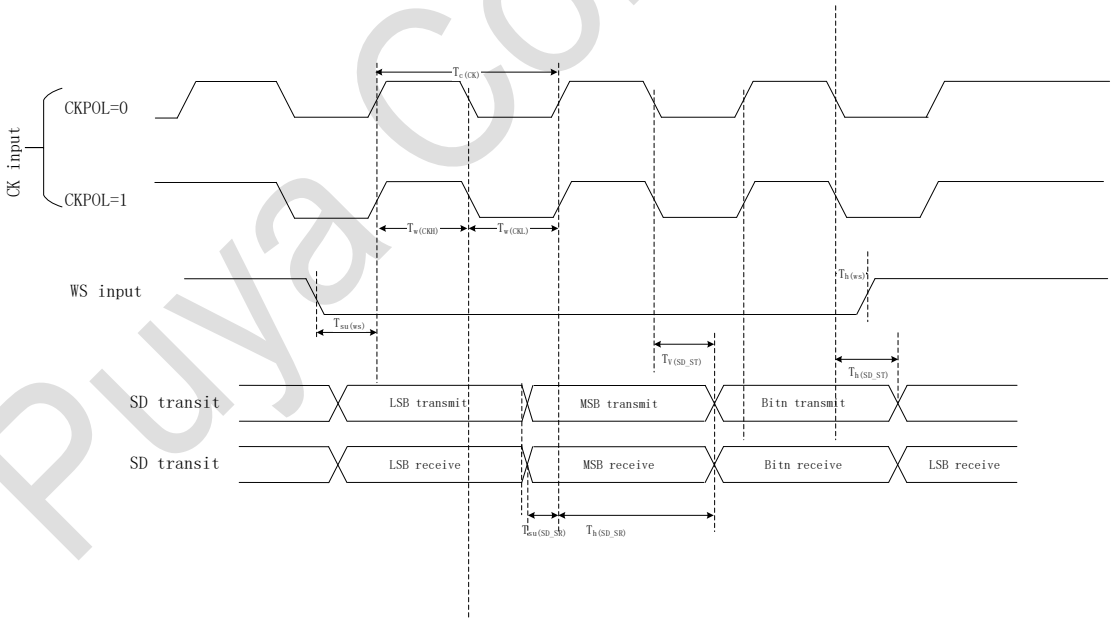


Figure 5-7 I²S slave timing diagram (Philips protocol)

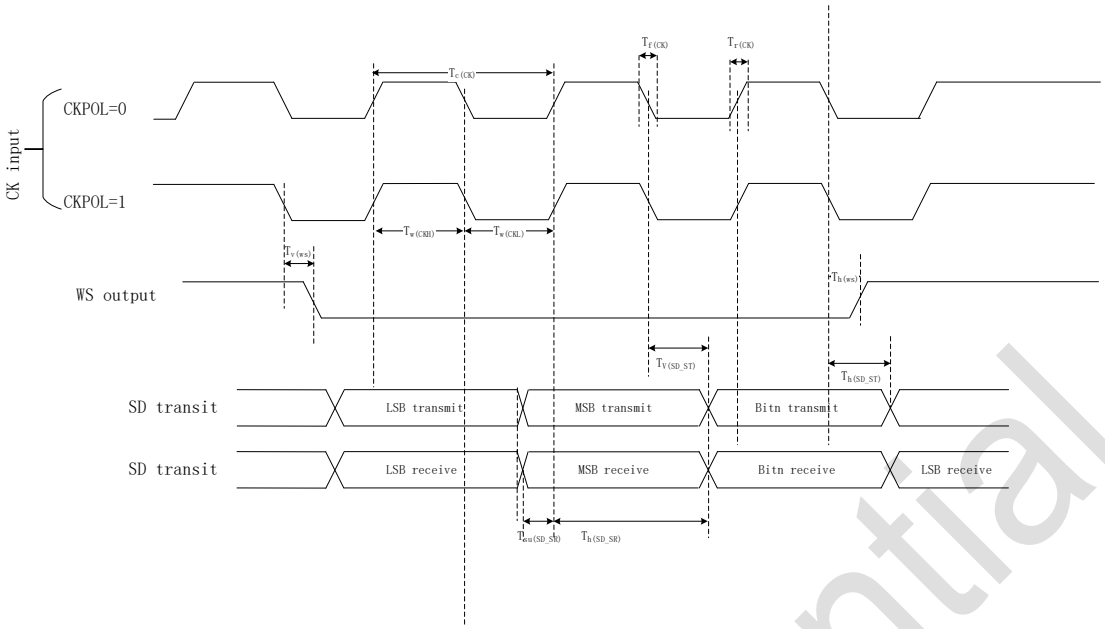


Figure 5-8 I²S master timing diagram (Philips protocol)

5.3.24.4. USB characteristics

Table 5-47 USB startup time

Symbol	Parameter	Max	Unit
t_{START}(1)	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 5-48 USB DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	USB transceiver operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(3)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	
V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(3)	Single ended receiver threshold	-	1.3	2	
Output voltage					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. The USB transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7 to 3.0 V V_{CC} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB drivers.

Table 5-49 USB OTG full speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L <= 50 pF	4	20	ns
t_f	Fall time(2)	C_L <= 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal.

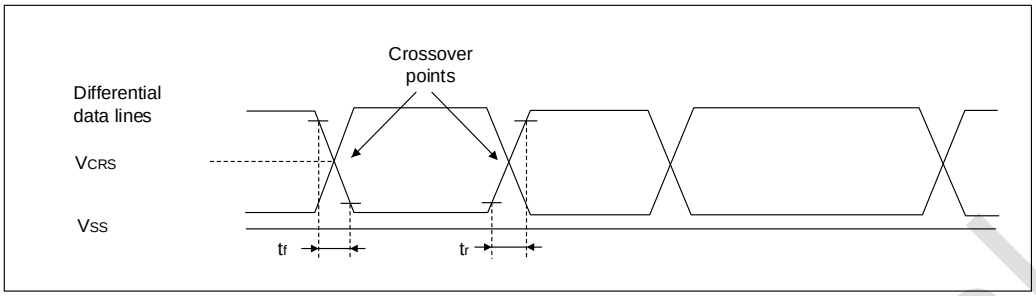


Figure 5-9 USB timing: data signal rise and fall time definition

5.3.24.5. ETH interface characteristics

Table 5-50 SMI characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle (1.67 MHz, AHB = 170 MHz)	-	600	-	ns
$t_{d(MDIO)}$	MDIO write data valid Time	13.5	14.5	15.5	ns
$t_{su(MDIO)}$	Read data setup time	35	-	-	ns
$t_{h(MDIO)}$	Clock low time	8.5	-	-	ns

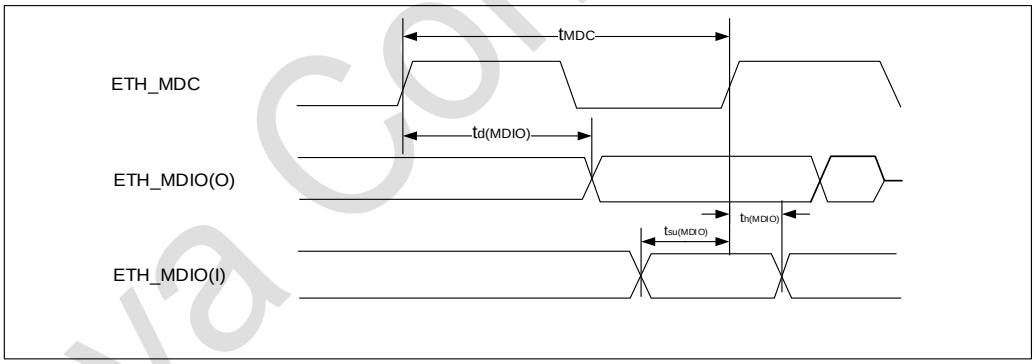


Figure 5-10 SMI timing figure

Table 5-51 RMII characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{h(RXD)}$	Data retention time	2	-	-	ns
$t_{su(DV)}$	Carrier sense build time	4	-	-	ns
$t_{h(DV)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmission effective delay enable time	8	10	16	ns
$t_{d(TXD)}$	Transmission effective delay time	7	10	16	ns

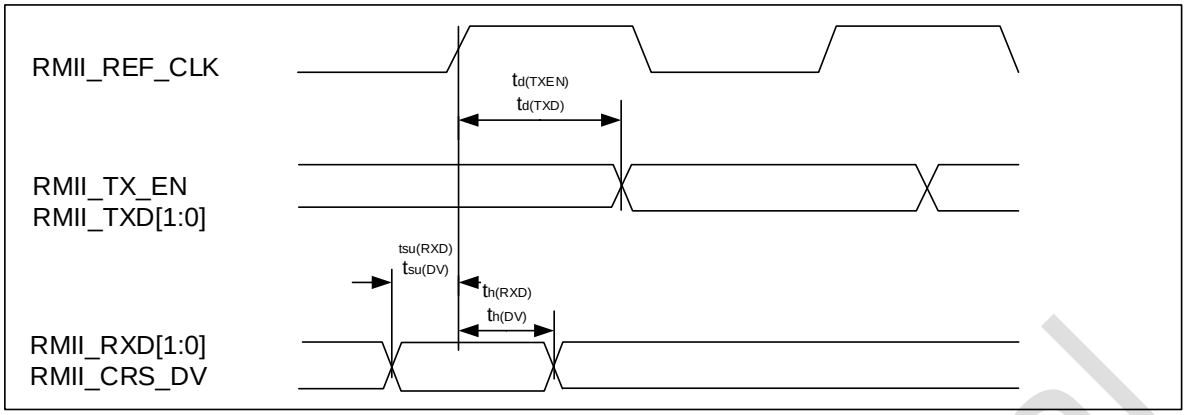


Figure 5-11 RMII timing Figure

Table 5-52 MII characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	MDC Cycle Establishment Time	10	-	-	ns
$t_{h(RXD)}$	Data retention time	10	-	-	ns
$t_{su(DV)}$	Carrier sense build time	10	-	-	ns
$t_{h(DV)}$	Carrier sense hold time	10	-	-	ns
$t_{su(ER)}$	Error establishment time	10	-	-	ns
$t_{h(ER)}$	Error hold time	10	-	-	ns
$t_{d(TXEN)}$	Transmission effective delay enable time	14	16	18	ns
$t_{d(TXD)}$	Transmission effective delay time	13	16	20	ns

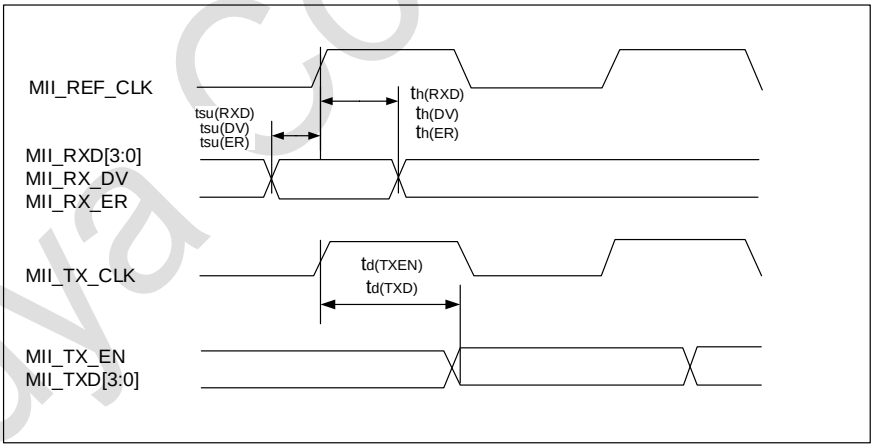


Figure 5-12 MII timing figure

5.3.24.6. LCD interface characteristics

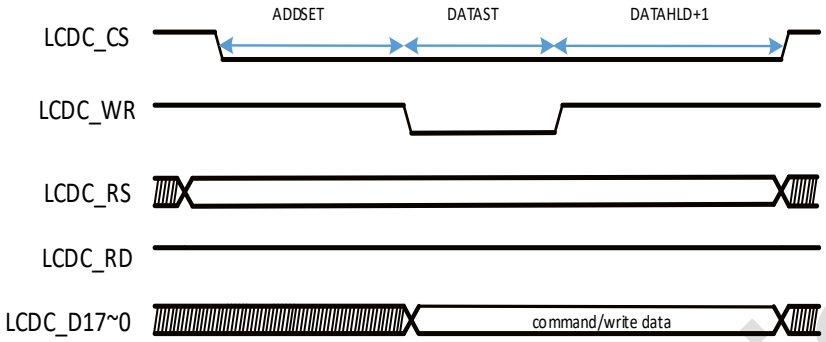


Figure 5-13 8080 mode write timing figure

Table 5-53 8080 mode write characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ADDSET}	Write operation 8080 address establishment time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$16t_{PCLK}$	-
t_{DATAST}	Write operation 8080 data setup time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$256t_{PCLK}$	-
$t_{DATAHLD}$	Write operation 8080 data hold time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$17t_{PCLK}$	-

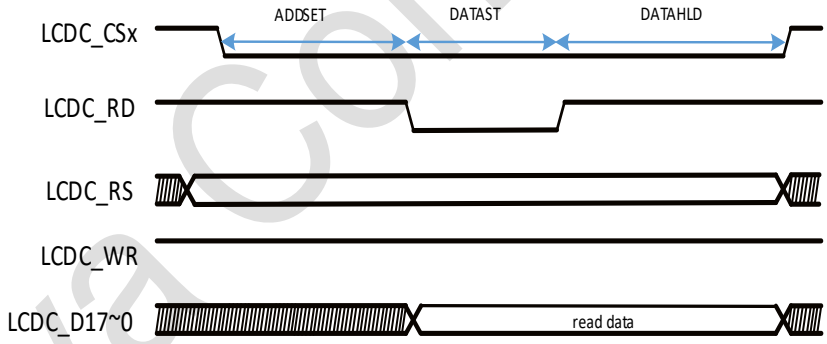


Figure 5-14 8080 Mode Read Timing Figure

Table 5-54 8080 mode read characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ADDSET}	Read operation 8080 address establishment time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$16t_{PCLK}$	-
t_{DATAST}	Read operation 8080 data setup time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$256t_{PCLK}$	-
$t_{DATAHLD}$	Read operation 8080 data hold time	8080 mode (MODEx=0)	$1t_{PCLK}$	-	$16t_{PCLK}$	-

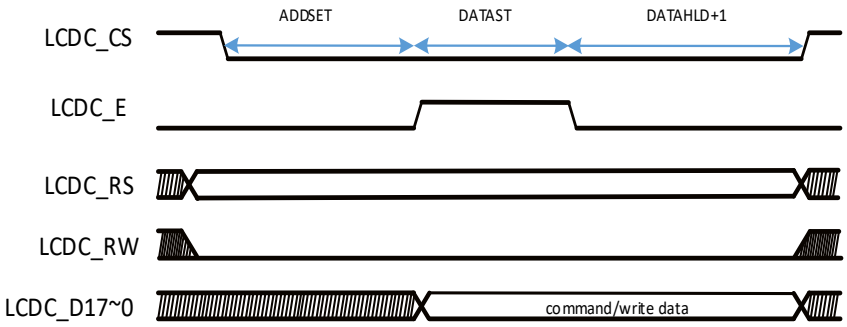


Figure 5-15 6800 mode write timing

Table 5-55 6800 mode write characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ADDSET}	Write operation 6800 address establishment time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$16t_{PCLK}$	-
t_{DATAST}	Write operation 6800 data establishment time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$256t_{PCLK}$	-
$t_{DATAHLD}$	Write operation 6800 data hold time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$17t_{PCLK}$	-

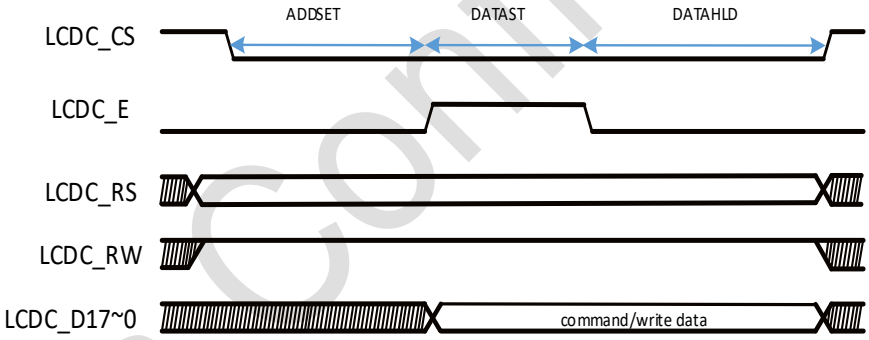


Figure 5-16 6800 mode read timing figure

Table 5-56 6800 mode read characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ADDSET}	Read operation 6800 address establishment time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$16t_{PCLK}$	-
t_{DATAST}	Read operation 6800 data establishment time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$256t_{PCLK}$	-
$t_{DATAHLD}$	Read operation 6800 data hold time	6800 mode (MODEx=1)	$1t_{PCLK}$	-	$16t_{PCLK}$	-

5.3.24.7. SD/SDIO MMC card host interface (SDIO) characteristics

Table 5-57 SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	C_L = 30 pF	0	48	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	-	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.3	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode					
t_{ISU}	Input setup time	f_{PP} = 48 MHz	3.5	-	ns
t_{IH}	Input hold time	f_{PP} = 48 MHz	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	f_{PP} = 48 MHz	-	7	ns
t_{OH}	Output hold time	f_{PP} = 48 MHz	3	-	
CMD, D inputs (referenced to CK) in SD default mode					
t_{ISUD}	Input setup time	f_{PP} = 24 MHz	1.5	-	ns
t_{IHD}	Input hold time	f_{PP} = 24 MHz	0.5	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	f_{PP} = 24 MHz	-	6.5	ns
t_{OHD}	Output hold default time	f_{PP} = 24 MHz	3.5	-	

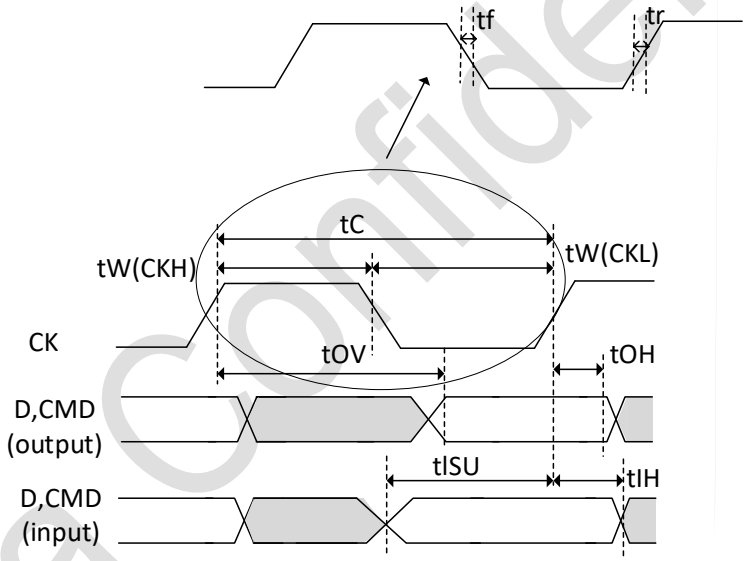


Figure 5-17 SDIO high-speed mode

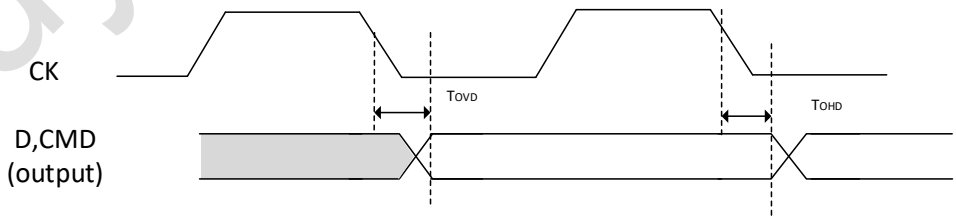


Figure 5-18 SDIO default mode

5.3.24.8. ESMC characteristics

Table 5-58 ESMC characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{QCK}	SPI clock frequency	2.3 < V_{CC} < 3.6 V	-	-	85	MHz
$t_{w(CKH)}$	Clock high level/low level time	2.3 < V_{CC} < 3.6 V	t_{QCK}/2-0.5	-	t_{QCK}/2+1	ns
$t_{w(CKL)}$			t_{QCK}/2-1	-	t_{QCK}/2+0.5	
$t_{s(IN)}$	Data input setup time	2.3 < V_{CC} < 3.6 V	1	-	-	
$t_{h(IN)}$	Data input hold time	2.3 < V_{CC} < 3.6 V	5	-	-	
$t_{v(OUT)}$	Data output valid time	2.3 < V_{CC} < 3.6 V	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	2.3 < V_{CC} < 3.6 V	0.5	-	-	

1. Evaluated by characterization, not tested in production.

Table 5-59 ESMC characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{QCK}	SPI clock frequency	2.3 < V_{CC} < 3.6 V	-	-	85	MHz
$t_{w(CKH)}$	Clock high level/low level time	2.3 < V_{CC} < 3.6 V	t_{QCK}/2	-	t_{QCK}/2+1	ns
$t_{w(CKL)}$			t_{QCK}/2-1	-	t_{QCK}/2+0.5	
$t_{sr(IN)}$	Data input setup time (rising edge)	2.3 < V_{CC} < 3.6 V	1	-	-	
$t_{sf(IN)}$	Data input setup time (falling edge)	2.3 < V_{CC} < 3.6 V	1	-	-	
$t_{hr(IN)}$	Data input hold time (rising edge)	2.3 < V_{CC} < 3.6 V	6	-	-	
$t_{hf(IN)}$	Data input hold time (falling edge)	2.3 < V_{CC} < 3.6 V	5	-	-	
$t_{vr(OUT)}$	Data output valid time (falling edge)	2.3 < V_{CC} < 3.6 V	-	7.5	8	
$t_{vf(OUT)}$	Data output valid time (rising edge)	2.3 < V_{CC} < 3.6 V	-	7	11	
$t_{hr(OUT)}$	Data output hold time (rising edge)	2.3 < V_{CC} < 3.6 V	2	-	-	
$t_{hf(OUT)}$	Data output hold time (falling edge)	2.3 < V_{CC} < 3.6 V	3	-	-	

1. Evaluated by characterization, not tested in production.

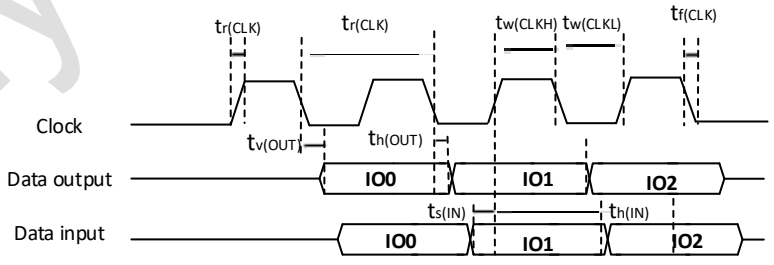


Figure5-19 ESMC timing diagram-SDR Mode

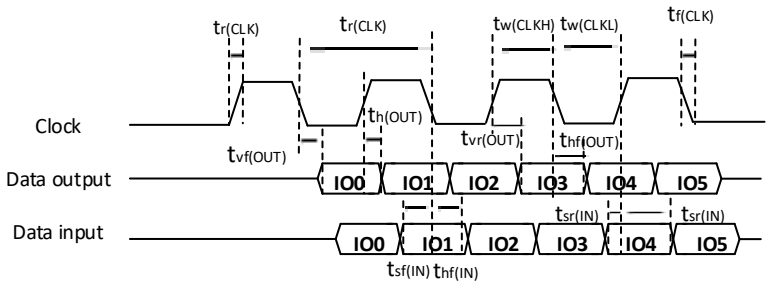


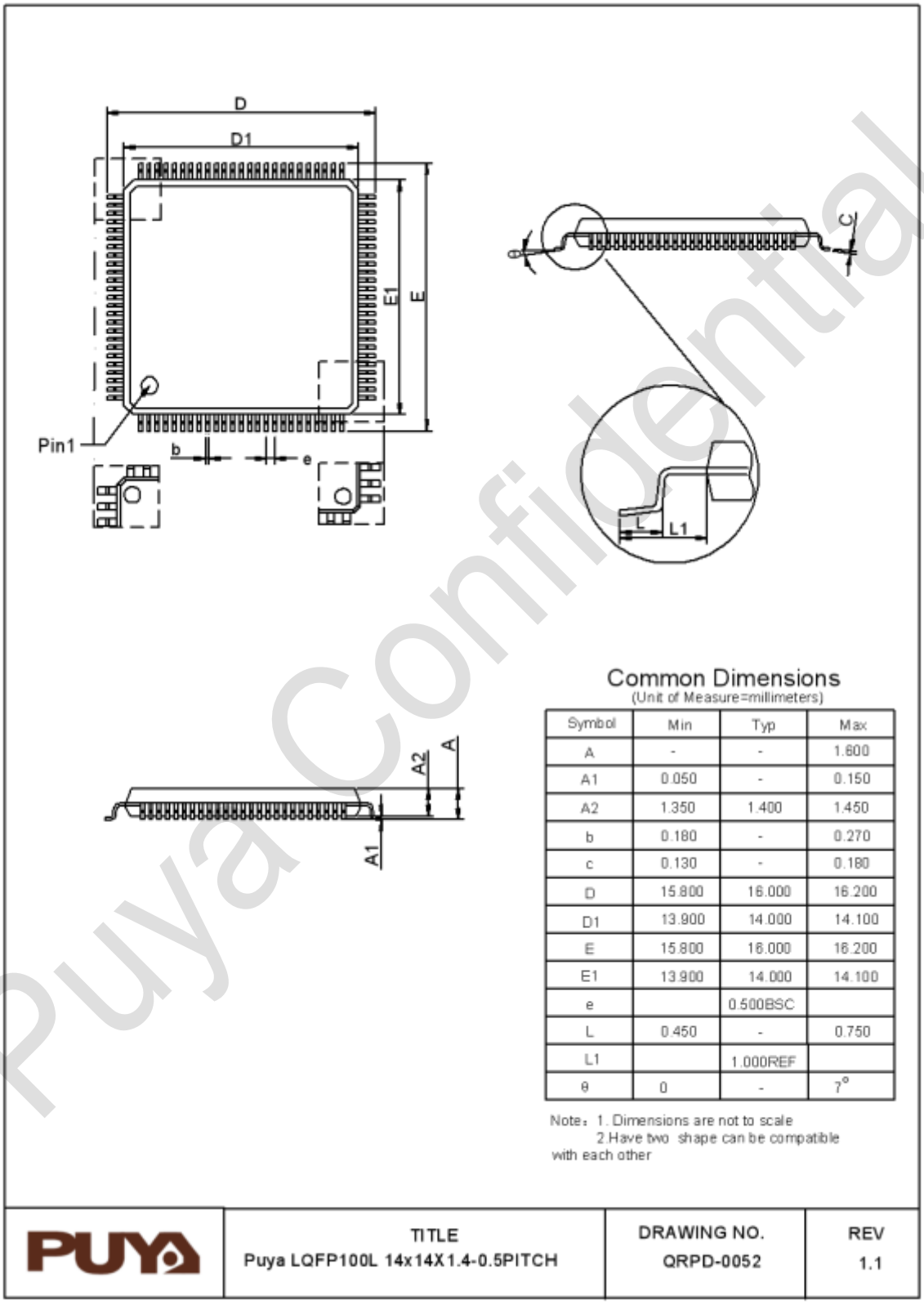
Figure5-20 ESMC timing diagram-DDR Mode

5.3.24.9. CAN 2.0 characteristics

Refer to Section I/O port characteristics for more details on the input/output alternate function characteristics

6. Package information

6.1. LQFP100 package size



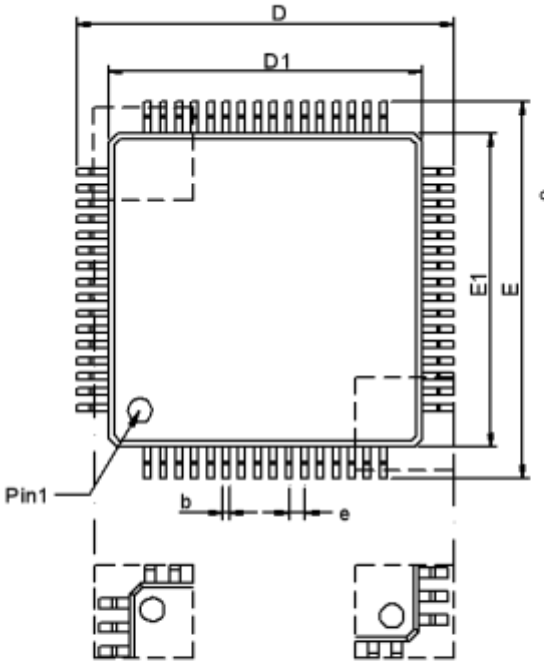
Common Dimensions
(Unit of Measure=millimeters)

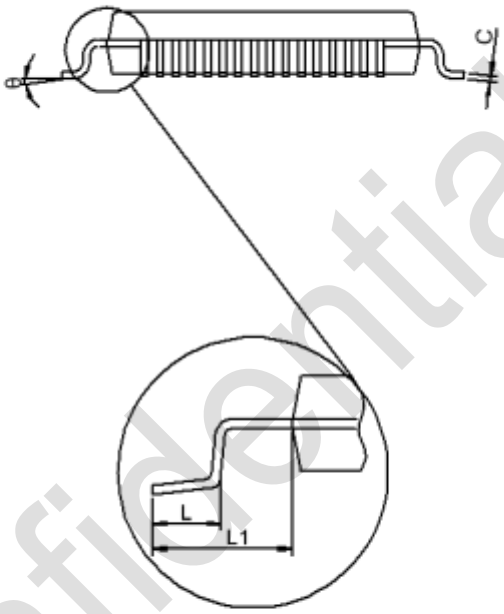
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	15.800	16.000	16.200
D1	13.900	14.000	14.100
E	15.800	16.000	16.200
E1	13.900	14.000	14.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

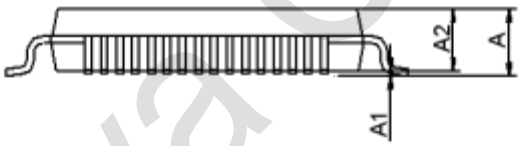
Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP100L 14x14X1.4-0.5PITCH	QRPD-0052	1.1

6.2. LQFP64 package size







Common Dimensions

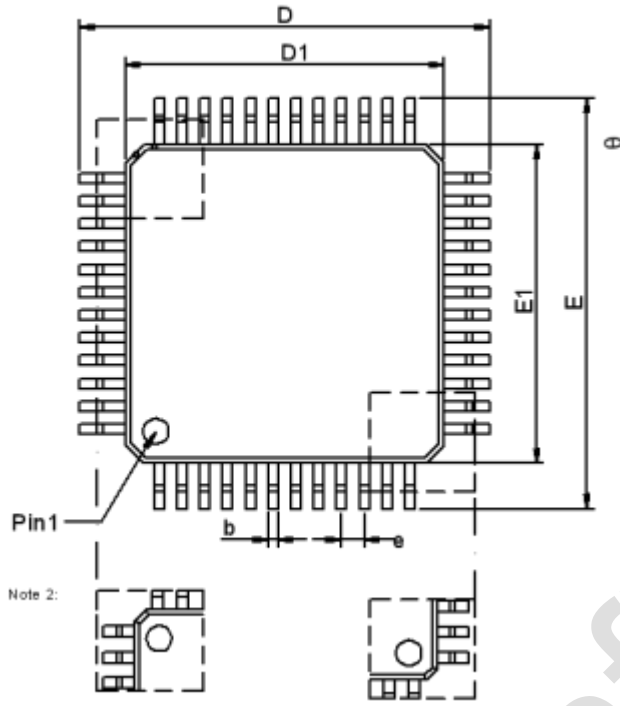
(Unit of Measure=millimeters)

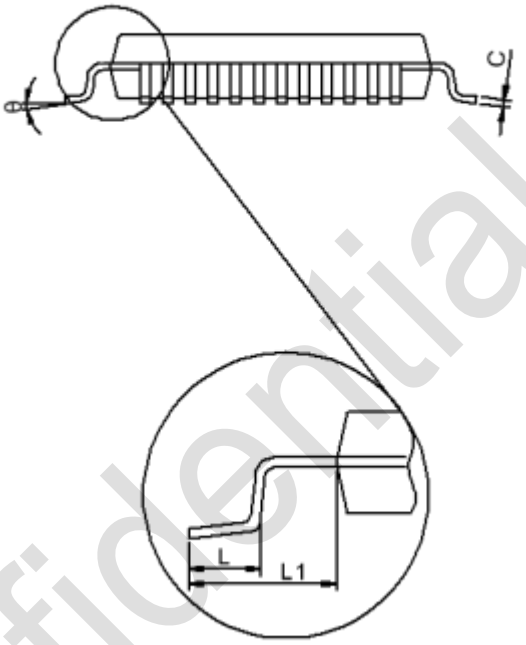
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	11.950	12.000	12.050
D1	9.900	10.000	10.100
E	11.950	12.000	12.050
E1	9.900	10.000	10.100
e		0.500BSC	
L	0.530	-	0.700
L1		1.000REF	
θ	0	-	7°

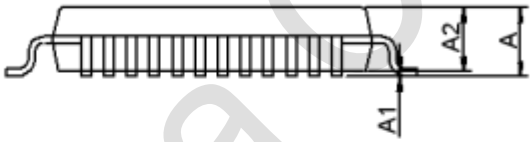
Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP64L 10x10X1.4-0.5PITCH	QRPD-0051	1.1

6.3. LQFP48 package size







Common Dimensions

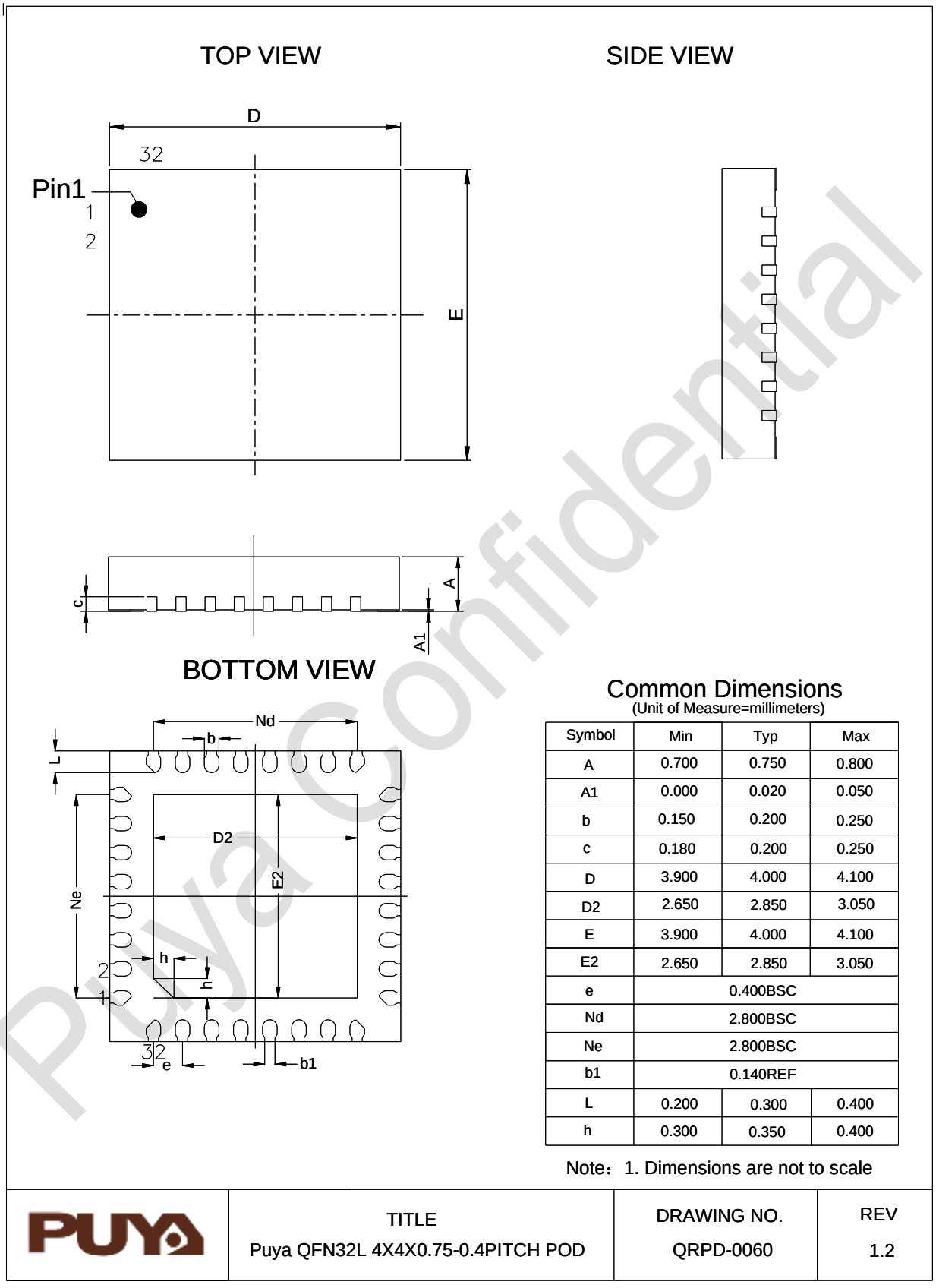
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

6.4. QFN32(4*4) package size



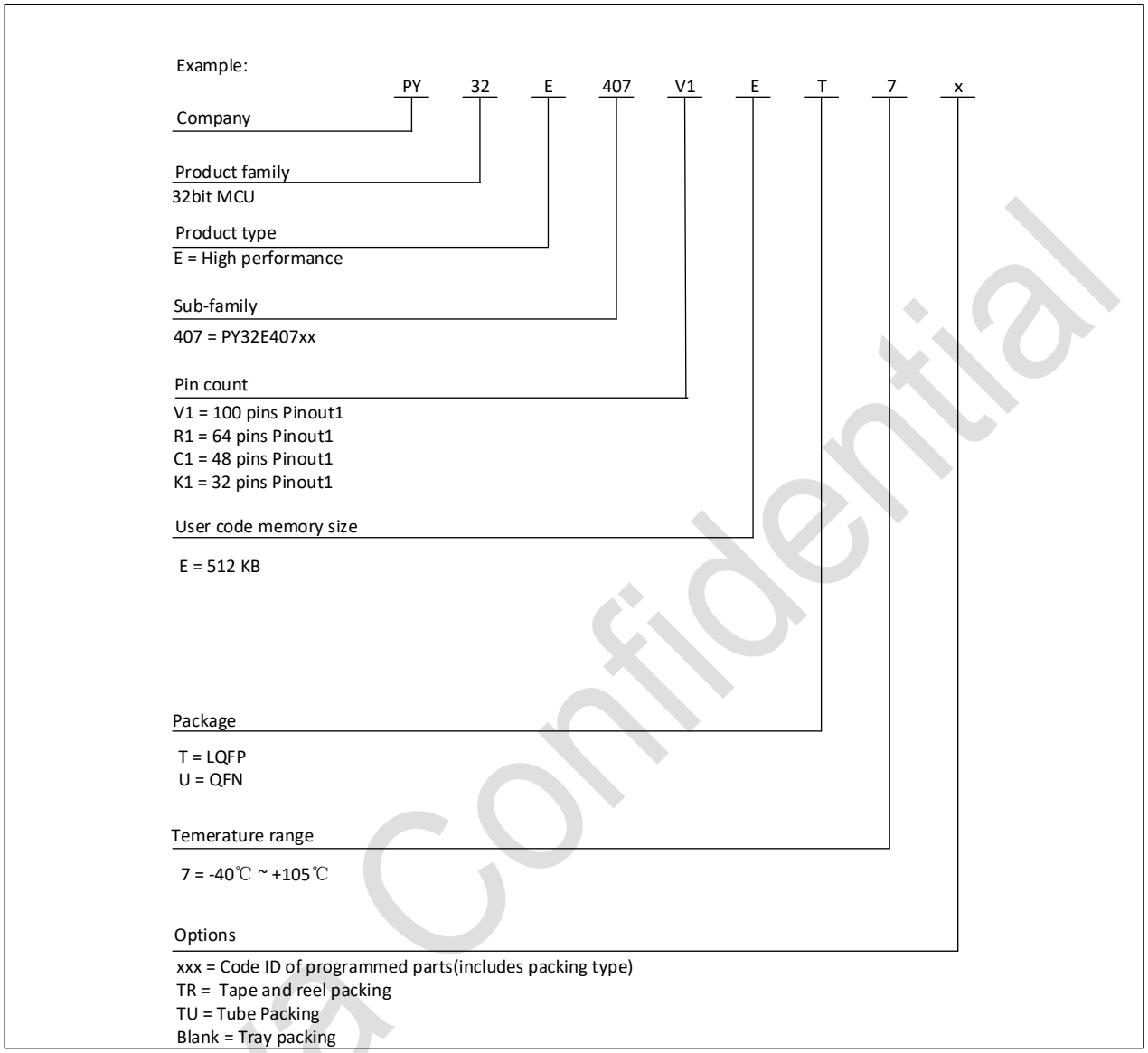
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

7. Ordering information



8. Version history

Version	Date	Descriptions
V0.5	2024.10.29	1. Initial version
V0.6	2024.11.04	1. Add QFN 32(4*4) Package
V0.7	2025.04.18	1. Update to version V1B 2. Add QFN48 package
V0.8	2025.04.25	1. Add HSE bypass function 2. Addition of IRTIM (infrared interface)
V0.9	2025.08.18	1. Update Table 3-2 Pin definitions
V0.10	2025.09.08	1. Update the number of USART

Puya Semiconductor Co., Ltd.