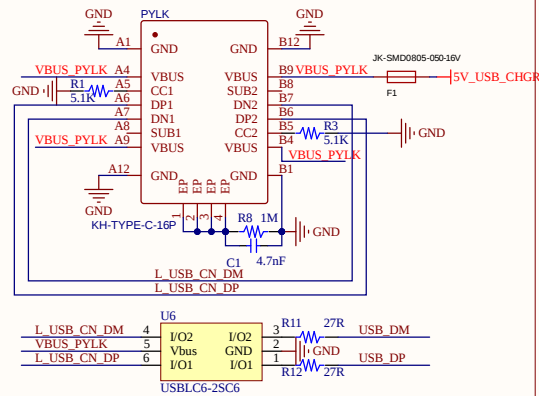
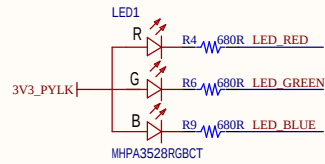


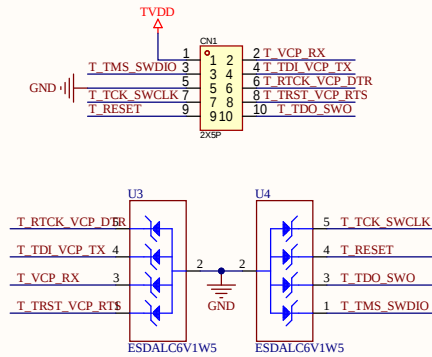
USB



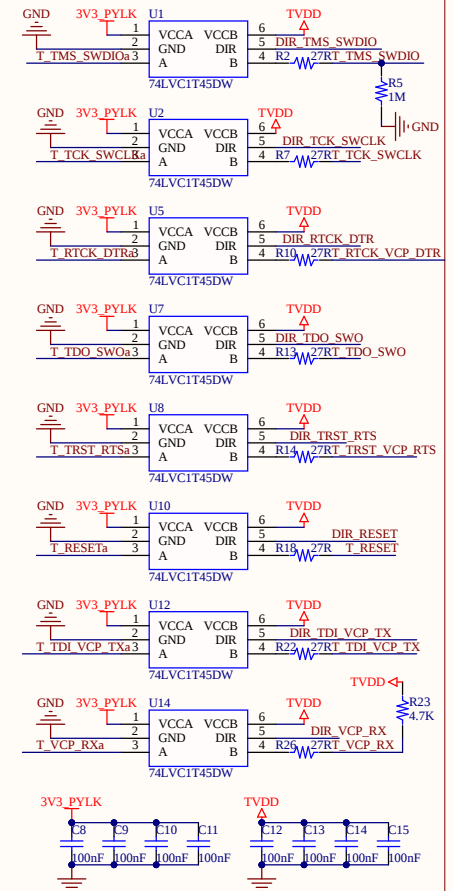
LED



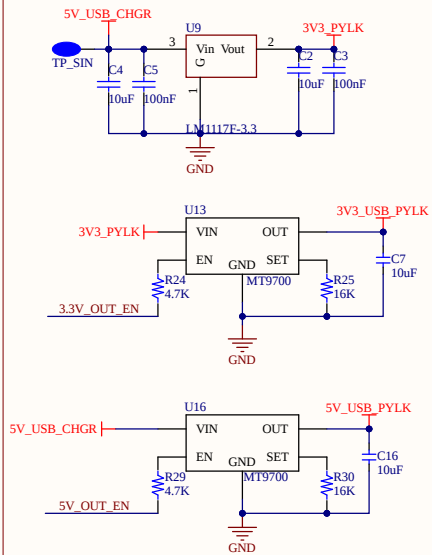
Debug Connector



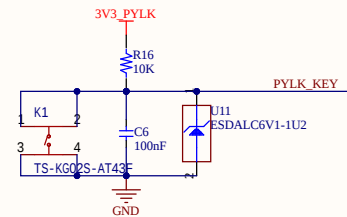
Level Shift



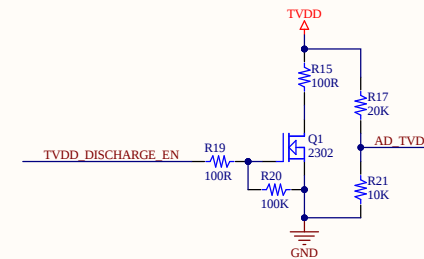
Power



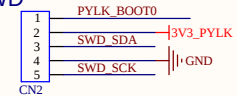
Key



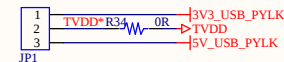
ADC&Electric discharge



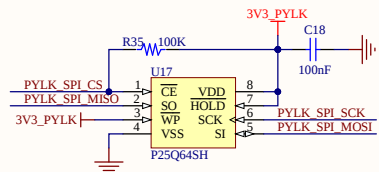
SWD



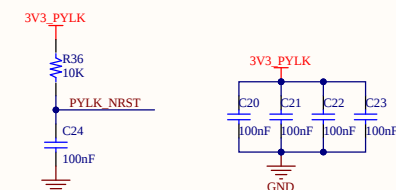
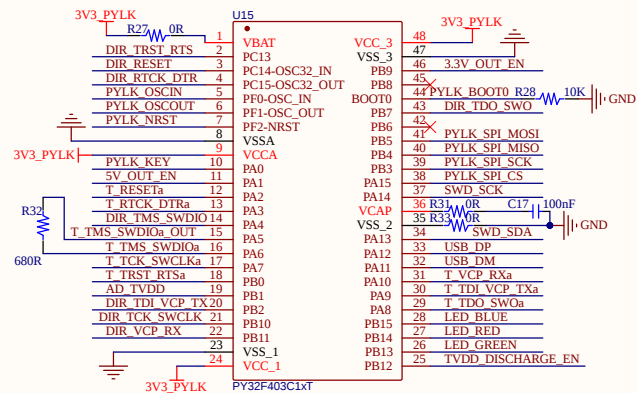
TVDD_Selection



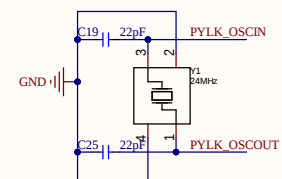
Flash



MCU



OSC



[D]P432E403V1X1[STAR]7[D]	T TMS SWDIO
[D]P432E403V1X1[STAR]7[D]	T TCK SWCLK
[D]P432E403V1X1[STAR]7[D]	T RESET
[D]P432E403V1X1[STAR]7[D]	T DTD SWO
[D]P432E403V1X1[STAR]7[D]	T VCP RX
[D]P432E403V1X1[STAR]7[D]	T TDI VCP TX
[D]P432E403V1X1[STAR]7[D]	T RTCK VCP DTR
[D]P432E403V1X1[STAR]7[D]	T RTST VCP RTS



OSC

GND

C27 22pF

C30 22pF

R38 0R

R41 0R

OSC_IN

OSC_OUT

Y2 24MHz

24MHz

PC14_OSC32_IN

PC15_OSC32_OUT

Y3 32.768KHz

C32 22pF

C33 22pF

R44 0R

R45 0R

32.768KHz

LED

The diagram shows a circuit for driving an LED from a microcontroller pin labeled PA1. The PA1 pin is connected to one terminal of a resistor labeled R54 with a value of 1K. The other terminal of the resistor is connected to the anode of a green LED. The cathode of the LED is connected to a terminal labeled TVDD. The LED is represented by a blue triangle pointing towards the TVDD terminal, with the word 'GREEN' written above it.

USB & POWER

Debug Connector

TVDD

CN3

1 2 3 4 5

Header 5

PA13 R37 100R T TMS SWDIO

PA14 R39 100R T TCK SWCLK

NRST R40 0R T RESET

GND

The diagram illustrates the BOOT_OPTION circuit. A 3x2 header is connected to a JP2 jumper. The connections are as follows:

- Pin 1: Connected to TVDD (5V).
- Pin 2: Connected to R43 (10K) resistor, which leads to BOOT0.
- Pin 3: Connected to PB2R42 (10K) resistor, which leads to GND.
- Pin 4: Connected to GND.
- Pin 5: Connected to GND.
- Pin 6: Connected to GND.

FLASH

The diagram shows a P25Q64SH flash memory chip with the following connections:

- Power:** F_VDD is connected to pin 8 via R46 (0R) to TVDD and to pin 7 via R47 (100K) to F_VDD. A 100nF capacitor C36 is connected between F_VDD (pin 7) and GND.
- Control:** F_CS is connected to pin 1, F_SO to pin 2, F_WP to pin 3, and GND to pin 4.
- Data:** F_HOLD is connected to pin 7, F_SCK to pin 6, F_SI to pin 5, F_PA2 to pin 8, F_PB10 to pin 7, F_PB1 to pin 6, F_PB0 to pin 5, F_PA7 to pin 4, and F_PA6 to pin 3.

3.3V PWR

The diagram shows a 3.3V PWR regulation circuit. A 5V input is connected to a fuse F2, then to the Vin pin of a voltage regulator U20 (LM1117F-3.3). The Vout pin of U20 is connected to the 3V3 output. Input capacitors C46 (10uF) and C47 (100nF) are connected to the Vin pin. Output capacitors C43 (10uF) and C44 (100nF) are connected to the Vout pin. The GND pin of U20 is connected to a common ground.

VDD_Selection

The diagram illustrates a circuit for VDD selection. A 3V3 source is connected to JP3. JP3 is connected to JP4. JP4 is connected to TVDD. JP4 is also connected to a 680R resistor (R65) which is connected to GND. JP4 is also connected to an OR gate. The OR gate is connected to LED1_VDD* which is connected to GND.

The diagram shows the NRST pin configuration. The NRST pin is connected to a 0R resistor (R58) and a pull-up resistor (R57, 10K) to TVDD. A diode (U21, ESDALC6V1-1U2) is connected between NRST and GND. A capacitor (C45, 100nF) is connected between NRST and GND. A TS-KG02S-AT43F temperature sensor is connected to GND and NRST.

5V_PWR_Selection

Title: PY32F403V1xT_START.SchDoc		
Project: PY32F403V1xT_START.PrjPcb		
Size: A3	Date: 2026/7/6	
Sheet: 2 of 2	Revision: V2.0	