Introduction

The PY32E407 series microcontroller uses high-performance 32-bit ARM ® Cortex ®- M4F Core MCU.Embedded with the Flash up to 512 Kbytes and the SRAM memory up to 144 Kbytes, and with the maximum operating frequency of 170 MHz. The PY32E407 contains multiple packaging types and products.

This document will help users understand the attentions for the application of various modules in PY32E407 and quickly start development.

Table 1 Applicable Products

Type	Product Series
Microcontroller Series	PY32E407

Contents

1 PWR Configuration

- To reduce the power consumption in STANDBY mode, it is recommended to configure the registers (PWR->CR1_SRAM_RETV, PWR->CR1_VOS) to 0x2 before entering STANDBY.
- Configuring the MCU to Standby mode through software needs 31 system clock cycles to completely enter the Standby mode. If an NRST reset or wake-up signal is generated, both the reset and wake-up will fail.

2 FLASH Configuration

- When using the RWW (Read-While-Write) feature, do not access BANK0 while erasing or writing to BANK0, and do not access BANK1 while erasing or writing to BANK1 (e.g., during erasure or writing to BANK0, the default interrupt vector entry is BANK0, so entering an interrupt is equivalent to accessing BANK0);
- When using the RWW (Read Write) function, the erase program must not be placed at the end of BANK0 (usually referring to the last SECTOR, which is about 4K);
- When using the PCROP (proprietary code read protection) function, due to incomplete correspondence between logical and physical addresses, the two high-order blocks (0x00840000~0x0805FFFF) cannot be protected when the FLASH size is 384K.

SIZE	Logical address	Logic Block No			Physical Block No
384K	0x0800 0000 - 0x0800 FFFF	1	BANK0	0x0800 0000 - 0x0800 FFFF	1
	0x0801 0000 - 0x0801 FFFF	2		0x0801 0000 - 0x0801 FFFF	2
	0x0802 0000 - 0x0802 FFFF	3		0x0802 0000 - 0x0802 FFFF	3
				0x0803 0000 - 0x0803 FFFF	
	0x0803 0000 - 0x0803 FFFF	4	BANK1	0x0804 0000 - 0x0804 FFFF	5
	0x0804 0000 - 0x0804 FFFF	5		0x0805 0000 - 0x0805 FFFF	6
	0x0805 0000 - 0x0805 FFFF	6		0x0806 0000 - 0x0806 FFFF	
				0x0807 0000 - 0x0807 FFFF	4
256K	0x0800 0000 - 0x0800 FFFF	1	BANK0	0x0800 0000 - 0x0800 FFFF	1
	0x0801 0000 - 0x0801 FFFF	2		0x0801 0000 - 0x0801 FFFF	2
				0x0802 0000 - 0x0802 FFFF	
				0x0803 0000 - 0x0803 FFFF	
	0x0802 0000 - 0x0802 FFFF	3	BANK1	0x0804 0000 - 0x0804 FFFF	
	0x0803 0000 - 0x0803 FFFF	4		0x0805 0000 - 0x0805 FFFF	
				0x0806 0000 - 0x0806 FFFF	3
				0x0807 0000 - 0x0807 FFFF	4
128K	0x0800 0000 - 0x0800 FFFF	1		0x0800 0000 - 0x0800 FFFF	1
				0x0801 0000 - 0x0801 FFFF	
				0x0802 0000 - 0x0802 FFFF	
				0x0803 0000 - 0x0803 FFFF	
	0x0801 0000 - 0x0801 FFFF	2		0x0804 0000 - 0x0804 FFFF	
				0x0805 0000 - 0x0805 FFFF	2
				0x0806 0000 - 0x0806 FFFF	
				0x0807 0000 - 0x0807 FFFF	

Figure 3-1 The correspondence between logical and physical addresses of BANK0 and BANK1

3 GPIO Configuration

- When only using Vbat pin to supply power, PC13 cannot be used.

4 Option Configuration

- When mass production, Option operation needs to be configured in the Option Byte configuration of the porgammer, and the function that operates Option in the program should be blocked.
- It is recommended that the customer program enables write protection, which is set in Option, as shown in Figure 5-1 and Figure 5-2.

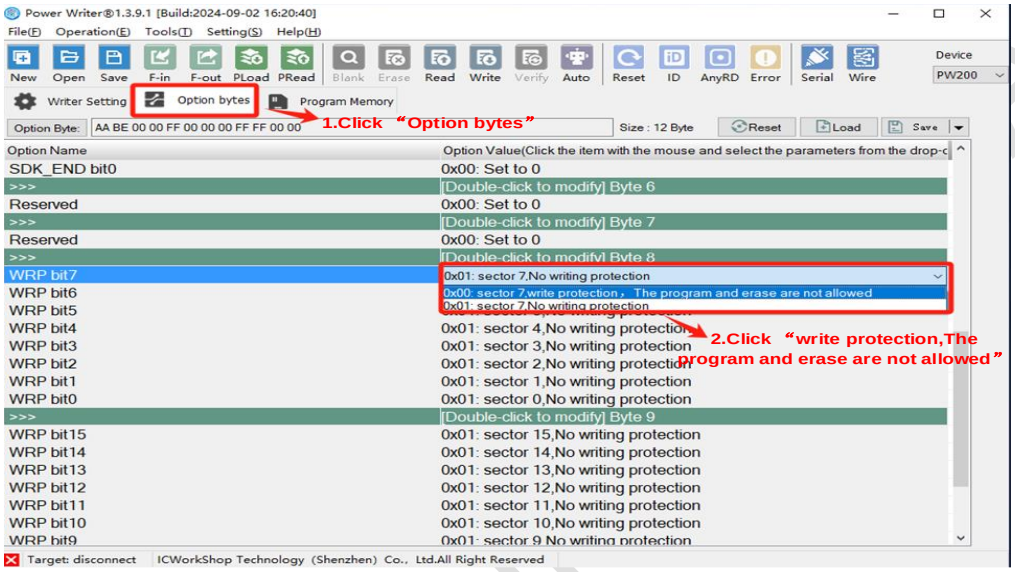

Figure 5-1 Power Write Operation Option Write Protection

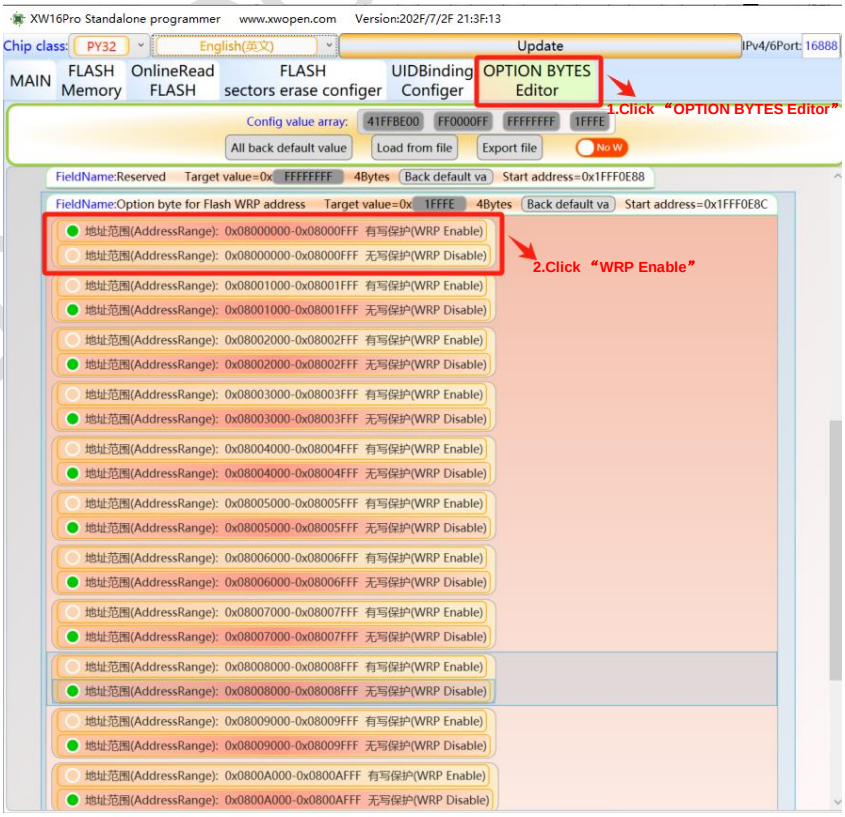

Figure 5-2 XW operation Option write protection

- When configuring the Option of the programmer, you need to check the "Smart Reset" function or "Restart the chip after programming" (programmers typically have similar options that need to be selected). The specific steps are shown in Figures 5-3, Figure 5-4.

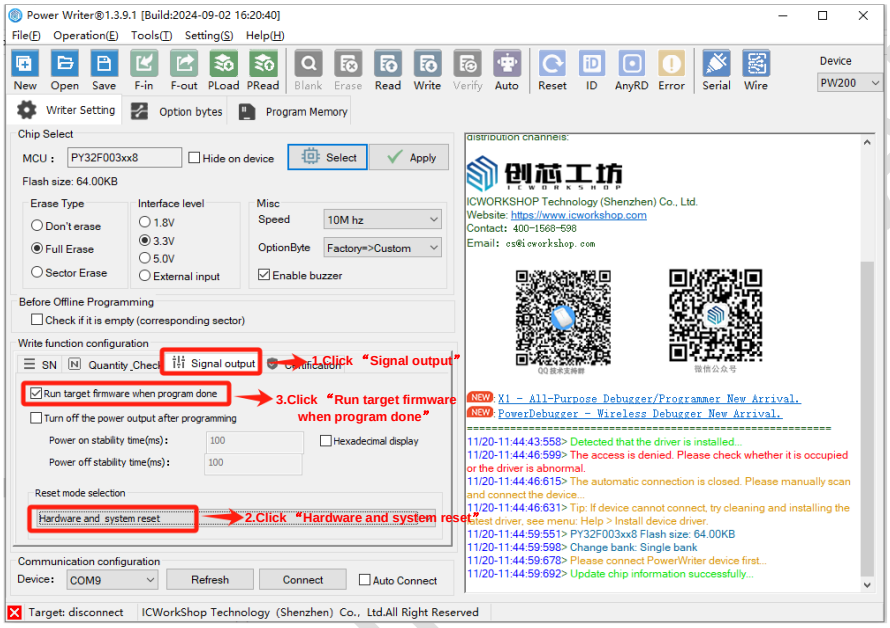

Figure 5-3 Power Write Operation Tick 'Reboot Chip After Programming"

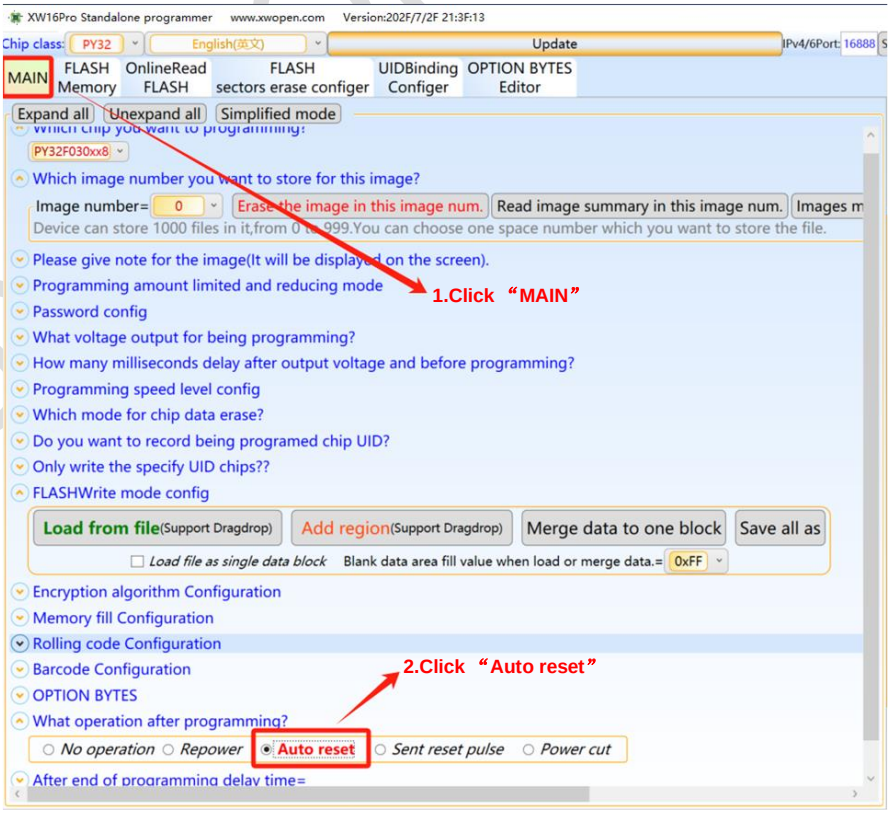

Figure 13-4 XW Operation ‘Smart Reset’

5 Version History

Version	Date	Update Records
V1.2	2025.10.23	Initial release
V1.3	2026.2.9	Delete RCC configuration

Puya Semiconductor Co., Ltd.